# B. Tech (Third Semester Computer Science \& Engineering (C.B.C.S)) Winter - 2022 <br> End Semester Examination <br> Course Name: Fundamentals of Digital Circuits \& Microprocessor 

Course Code: BCS2302
ASD/EFV5/63-5F/1471
Time: 3 Hours]
[Max. Marks: 60

## Instructions to Candidates:

1. All questions carry marks as indicated.
2. All the sub- questions ( $a, b, c, d$, and e) ofQue. 1 in Section $A$ are compulsory.
3. Solve any two sub-questions in Que. 2 to Que. 6 in Section B.
4. Assume suitable data wherever necessary.
5. Use of non-programmable calculator is permitted.

## Section A

Que. 1. (a) Convert hexadecimal number (A0F9.0EB) 16 into decimal form.
(b) Convert the Boolean expression $\mathrm{Y}=\mathrm{AB}+\mathrm{A} \mathrm{B}^{\prime} \mathrm{C}+\mathrm{BC}^{\prime}$ into
standard Boolean SOP expression.
(c) Distinguish between combinational and sequential circuits.
(d) Illustrate race around condition for $\mathrm{J}-\mathrm{K}$ flip flop.
(e) Write different features of 16-bit Microprocessor 8086 .

## Section B

Que. 2. (a) Explain and verify De-Morgan's theorem using suitable example.
(b) Write short notes with example:
i) XS-3 code
ii) Gray code
(c) Modify following Boolean expression with reduced number of mean terms.
i) $\mathrm{Y}=\mathrm{A}\left[\mathrm{B}+\mathrm{C}^{\prime}\left(\mathrm{AB}+\mathrm{AC}^{\prime}\right)^{\prime}\right]$
ii) $\mathrm{Y}=\left[\mathrm{A}+(\mathrm{BC})^{\prime}\right]^{\prime} \cdot\left[(\mathrm{AB})^{\prime}+\mathrm{ABC}\right]$

Que. 3. (a) Determine reduced SOP expression for the following and implement using logic gates,

$$
F(A, B, C, D)=\sum m(5,6,7,12,13)+d(4,9,14,15)
$$

(b) Write the following Boolean expression in standard SOP and canonic 5 form
$\mathrm{Y}=\mathrm{A}^{\prime} \mathrm{B}^{\prime} \mathrm{D}+\mathrm{A}^{\prime} \mathrm{B}+\mathrm{ABC}+\mathrm{ACD}{ }^{\prime}$
(c) Determine reduced POS expression for the following and implement using logic gates,

$$
F(A, B, C, D,)=\prod M(0,1,4,5,7,10,11,13,14,15)
$$

Que. 4 (a) Design Full adder using XOR and AOI logic gates.
(b) Show that Full subtractor can be designed using two half subtractor.
(c) Design 8:1 MUX using 4:1 MUX.

Que. 5. (a) Convert the S-R flip flop into J-K flip flop.
(b) Design and implement using JK flip flop negative edge triggered, 3-bit asynchronous up counter.
(c) Classify different types of RAM and explain each in brief.

Que.6. (a) Discuss on functioning of ALU and various registers of $8085 \quad 5$ (CO5) Microprocessor.
(b) Demonstrate different addressing modes of 8085 with one example for each.
(c) Sketch memory read timing diagram of 8085 Microprocessor and summarize sequence of operations in it.

