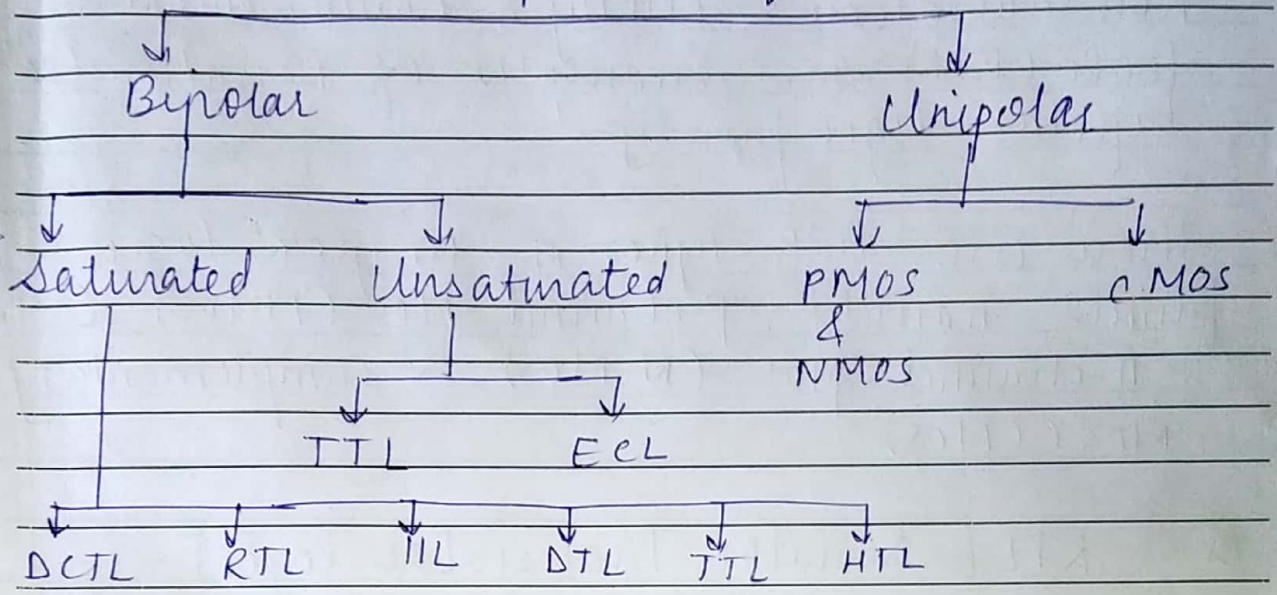
Unit 1

⋆ classification of logic family



The digital logic family has broadly classified into two types namely bipolar and unipolar. The bipolar logic families are classified as saturated & Non-saturated types.

In saturated type of bipolar logic family transistor are operated in between cut off and saturation.

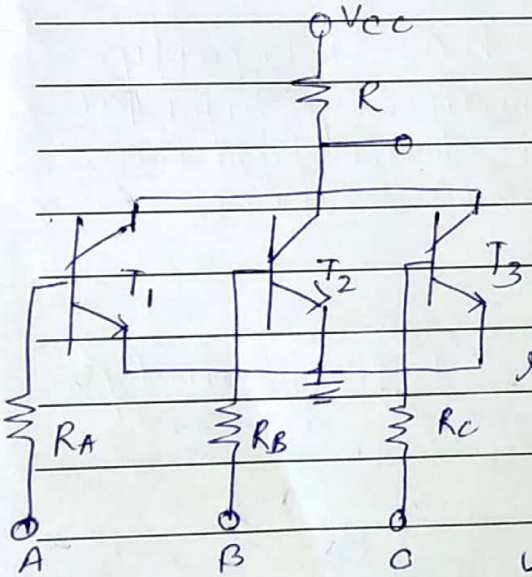
Resistor transistor logic (RTL), (DCTL) Direct coupled transistor logic, (IIL or I^2L) Integrated Injection logic, (DTL) Diode transistor logic), (TTL) transistor transistor logic & (HTL) High Threshold logic

are commonly used bipolar logic families.

In unsaturated bipolar logic family the transistor are operated in Beta cut off & non saturation. Schotty & Emitter coupled logic (ECL) are examples of unsaturated bipolar logic family.

There are two types of unipolar logic family namely p-channel MOS (PMOS) & n-channel MOS (N-MOS) & complementary MOS (CMOS).

⭐ RTL (Resistor Transistor logic).



RTL ckt of three I/P NOR gate is shown in fig. In this ckt resistance is connected in series with base of each transistor to reduce hogging current effect.

Actually the I/P capacitance has been charged & discharged through this additional resistance & time constant will be increased.

As its name suggest RTL ckt mainly consist of resistors & transistors.

Therefore the switching speed becomes slower. The fan out of RTL is four or five time delay is approximately 50 ns. ie(low)

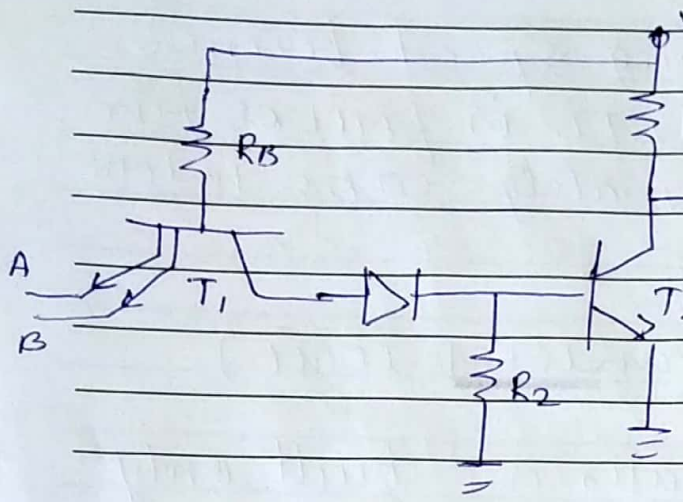
⑧ TTL (Transistor transistor logic)

In TTL logic gates are built only around transistors. TTL was developed in 1965. All TTL families are available in small scale integration (SSI) package and in more complex forms as MSI & LSI packages. The difference in TTL series are not in digital functions that they perform but rather in the values of resistance & different type transistor which are used to develop basic gates.

The family of TTL is standard TTL, High speed TTL, low power TTL, schottky TTL.

TTL ckt is most popular in bipolar logic family as it is fastest saturating logic family

Fig shows basic TTL ckt for a two i/p NAND gate. A single multi emitter transistor replaces i/p diodes serves as one i/p, and the base collector



diode function as the series diode.

The multi emitter transistor is economically fabricated in monlithic form. In this a single isolated collector region is diffused, A single base region is diffused & formed in the collector region and the several emitter region are diffused as seperate areas into the base Region

Fan Out : No of loads the o/p of a gate can drive w/o effecting its usual performance.

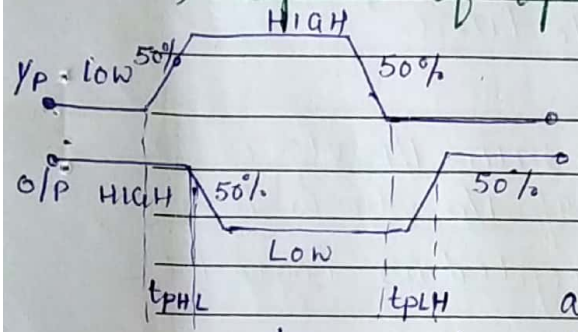
By load we mean the amt of current required by the i/p of another gate connected to the o/p of given gate

★ Characteristics of Digital logic family

The important performance parameters are given below

1) Speed of Operation 2) Power Dissipation
3) Vtg parameters 4) Current Parameters
5) Noise Immunity 6) Availability
7) Fan In 8) Fan Out 9) Cost

a) **Speed of operation:** The operating speed of a logic family is determined from the propagation delay. If a square wave is applied to I/P of an inverter, O/P of the inverter will be a square wave as shown in fig. It is very clear from fig that propogation delay is measured from the time difference betn 50% logic transition of I/P from its initial value & 50% logic transition of O/P. There are two types of propogation delay time t_{PHL}, t_{PLH}



t_{PHL} is delay time when O/P changes from High to low
t_{PLH} is delay for O/P when changes from low to High

Generally t_{PHL}, t_{PLH} are very close to each other

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⊙ Power Dissipation: It is the amount of power drawn from supply during static & dynamic condition. In the static condition, the power dissipated in a logic gate is also static power consumption & similarly dynamic power consumption takes place in dynamic condition or switching transitions. Static power consumption is power dissipated in logic gate when device is either ON or OFF. During transition from OFF to ON or ON to OFF the power consumed in a gate is called dynamic power consumption. It is directly proportional to switching freq & inversely proportional to cycle time.

⊙ Voltage parameters:

High level I/P vtg (V_{IH}): V_{IH} is min I/P vtg to be recognised as logic 1 or High. If I/P vtg is less than V_{IH} it will not be accepted as logic 1 or High.

Low level I/P vtg (V_{IL}): V_{IL} is max I/P vtg to be recognised as logic 0 or Low. When I/P vtg is greater than V_{IL} it will not be accepted as logic 0 or Low.

High level O/P vtg (V_{OH}): V_{OH} is min O/P vtg for High state or logic 1 under defined load condition.

Low level O/P vtg (V_{OL}): V_{OL} is max O/P vtg for low state or logic 0.

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- I_{OL} is the max current that O/P can sink in low state or logic 0.

⑤ Current Parameters: High level I/P current (I_{IH}):

I_{IH} is current that flows into an I/P when High level or logic 1 vtg is applied to that I/P.

low level I/P current (I_{IL}): I_{IL} is current that flows into an I/P when low level or logic 0 vtg is applied to that I/P.

I_{OH} is the max current that flows from an O/P & O/P can source in High state or logic 1.

⑥ Noise Immunity: Noise is alway present in electronics ckt due to stray & magnetic field. Sometimes it distorts the O/P vtg of gate. It means the ckt ability to tolerate noise. In order to recognise logic 0 or 1, noise immunity is measured quantitatively which is known as noise margin (NM). Two types of it are.

1) Low Noise immunity (LNM): V_{NL} is the largest noise amplitude that is for no change of O/P Vtg level when I/P vtg of logic gate is Low interval; $V_{NL} = V_{IL} - V_{OL}$.

2) HIGH NOISE MARGIN (HNM): V_{NH} is largest noise amplitude that is guaranteed for no change of O/P vtg level when I/P vtg of logic gate is High

$V_{NH} = V_{OH} - V_{IH}$.

⑦ Fan in: Fan in is the max no of I/P for a logic gate in a particular logic family. This no is limited due to delay time. For ex a two I/P AND gate has fan in of two, a three I/P OR gate has fan in of three, a NOT gate has fan it of one. Generally delay of operation of any gate increases with increasing fan in respectively

④ Fan Out : Fan out is defined as no of similar logic gates driven by a single logic gate. While a logic gates has high fan out.

Fan out depends on amount of source or sinks current of a gate while a logic gate has o/p ~~high fan out~~. with more than its rated fan out.

⑤ Cost : Cost of digital IC depends on quantity ~~measured~~ manufactured. The designer always tries to design low cost IC through quantity of IC used is large.

⑥ Availability : To choose a logic family for particular application, availability is an important parameters. Availability can be considered into different ways

1) popularity of logic family

2) Wired logic capability

3) Availability of complement o/p

4) Breadth of logic family

(A) Propagation Delay: When I/P to a gate changes suddenly, TTL gate response to I/P signal & it takes finite time to change the O/P state. This is due to change the switch from cut off state to saturation state or vice versa. The time delay is clas propogation delay. The switching times of BJT is also klas propogation delay.

(B) Delay time (td): When I/P Vtg suddenly changes at time t0, there is no change at O/P until time t_1. Here t_1 is the time when O/P Vtg start to decrease due to change in collector current. The delay is generated as Vtg across emitter & collector junction do not change instantaneously due to junction capacitance at the depletion region

(C) Fall time (tf): Due to junction capacitance effects, the output voltage decreases as depicted in fig

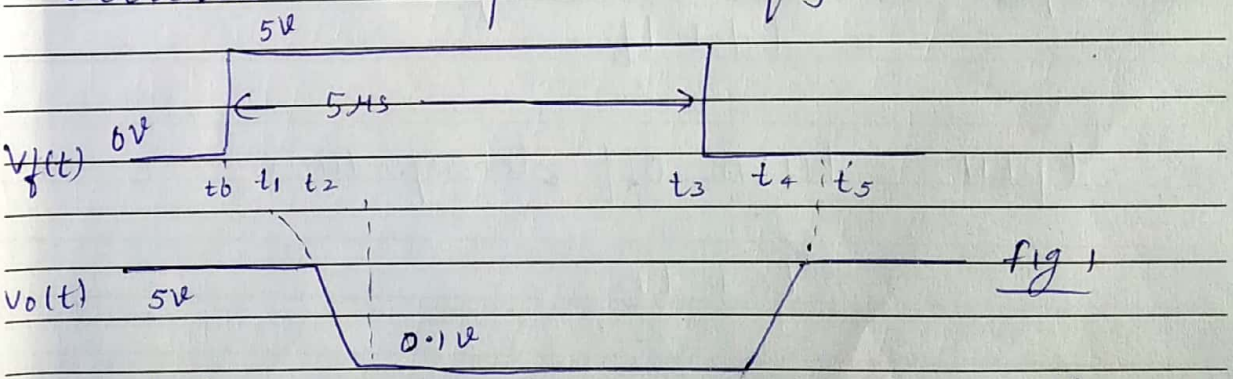

fig 1

At time t_2 the transistor is at the

fall time is $(t_2 - t_1)$

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edge of saturation & o/p vtg of transistor is 0.1v

⑤ Saturation Time (t_s): It is clear from fig 1 that there is another step change in i/p vtg from 5v to 0v at time t_3. i/p vtg changes suddenly, o/p vtg does not change till t_4 due to removal of overdrive charge from base & collector regin saturation time is computed as $(t_4 - t_3)$

⑥ Rise time (t_{rb}): Due to junction capacitance effects o/p vtg rises similar to fall time & the transistor is now turning off. At time t_5 the transistor is at edge of cut off. Consequent the o/p is V_{cc} is 5v. The rise time is difference betn t_5 & t_4.

The average propogation delay is defined as

$$t_p = \frac{t_{pHL} + t_{pLH}}{2}$$

where

t_{pHL} = Turn on delay time

$$= t_d + \frac{t_f}{2}$$

t_{pLH} = turn off delay time

$$= t_s + \frac{t_{rb}}{2}$$

(A) Combinational logic : A digital ckt is a combinational if its o/p is depending on i/p. It is memoryless. It deal with method of combining basic gates to get desired soln.

Combinational logic ckt can be constructed using logic gates & w/o fld from o/p to i/p

1) Product term : A product term is logical product (AND) of literals. for ex X, $X\bar{Y}$, XYZ are product of terms, where X, Y are boolean variables

2) Sum term : It is sum of literals or OR of literals for ex $X+\bar{Y}$, $X+Y+Z$ are sum terms

3) Sume of Products (SOP): It is logical exp in which OR of multiple product terms are present. SOP exp is $Y+X\bar{Y}+XYZ$

4) Products of sum (POS): It is logical exp in which AND of multiple OR terms are present. Exp is $(X+X\bar{Y})(XY+Z)(\bar{Y}+Z)$ is POS exp

5) Minterms: It is special type of product (AND) term. It is a product term which contains all the i/p variables that makes up a boolean exp

6) Maxterms: It is special type of OR term. It is sum term that contains all I/P variables that makes up a boolean exp.

7) Canonical Sum of Products: It is a complete

8) Canonical Product of Sum:

(*) Canonical Sum of Product (SOP) OR Minterm Representation and (POS) Product of Sum (Maxterm) representation.

In SOP (Sum of Product), the word sum and product are derived from symbolic representation of the OR and AND function respectively.

A product term is group of literals that are ANDed together. Eg ex ABC, XY etc

A sum term is any group of literals that are ORed together such A+B+C etc.

A sum of products (SOP) is a group of product terms ORed together. Ex are

1) $ABC + A\bar{B}\bar{C}$
2) $XY + XY\bar{Z} + YZ$

In SOP, we find minterms in which

$$0 = \bar{A}$$
$$1 = A$$

it is represented by Σm.

where,

Σ represents Sum of product

In POS, it is any group of sum terms ANDed together. some examples of this form are

1) $(A+B)(B+\bar{C})$

2) $(A+\bar{B}+C)(B+C+\bar{D})$

Each of these product of sums expressions consists of two or more sum terms (OR) that are ANDed together. Each sum term consists of one or more literals appearing in either complemented or uncomplemented form.

In POS, we find max terms in which

$0 = A$

$1 = \bar{A}$

It is represented by πM where

π represents product of sum.

⑧ Converting expression in standard SOP or POS form.

Sum of product form can be converted to standard sum of product by ANDing the term in the exp with terms formed by ORing the literal and its complement which are not present in that term.

For example for a three literal expression with literals A, B and C if there is a term AB, where C is missing then we form term $(C+\bar{C})$ and AND it with AB.

Therefore we get $AB(C+\bar{C}) = ABC + AB\bar{C}$

Q. Convert the given expression in standard SOP

$$Y = AC + AB + BC$$
$$= AC(B+\bar{B}) + AB(C+\bar{C}) + BC(A+\bar{A})$$
$$= ABC + A\bar{B}C + ABC + AB\bar{C} + ABC + \bar{A}BC$$
$$= ABC + A\bar{B}C + AB\bar{C} + \bar{A}BC.$$

as $(A+A = A)$

Q Convert the exp in standard SOP form

$Y = A + AB + ABC$

$= A(B+\bar{B})(C+\bar{C}) + AB(C+\bar{C}) + ABC$

$= (AB + A\bar{B})(C+\bar{C}) + ABC + AB\bar{C} + ABC$

$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + ABC$
$+ AB\bar{C} + ABC$

$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C}$

as $(A+A=A)$.

Q Convert the exp in standard POS form.

$Y = (A+B)(B+C)(A+C)$

$= (A + B + C\bar{C}) + (B + C + A\bar{A}) + (A + C + B\bar{B})$

$= (A+B+C)(A+B+\bar{C})(A+B+C)$

$(\bar{A}+B+C)(A+B+C)(A+\bar{B}+C)$.

$= (A+B+C)(A+B+\bar{C})(A+\bar{B}+C)$

as $A \cdot A = A$ $(\bar{A}+B+C)$.

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Q8. Convert the given exp in standard Pos form

$Y = A(A+B)(A+B+C)$

$= (A+B\bar{B}+C\bar{C})(A+B+C\bar{C})+(A+B+C)$

$= (A+B\bar{B}+C)(A+B\bar{B}+\bar{C})(A+B+C)$

$(A+B+\bar{C})(A+B+C)$

$= (A+B+C)(A+\bar{B}+C)(A+B+\bar{C}) =$

$(A+\bar{B}+\bar{C})(A+B+C)(A+B+\bar{C}) =$

$(A+B+C).$

$= (A+B+C)(A+B+\bar{C})(A+\bar{B}+C)$

$(A+\bar{B}+\bar{C})$

☆ SOP (Sum of Product) / Minterms Representation (1)

for two variable

Truth table is shown below

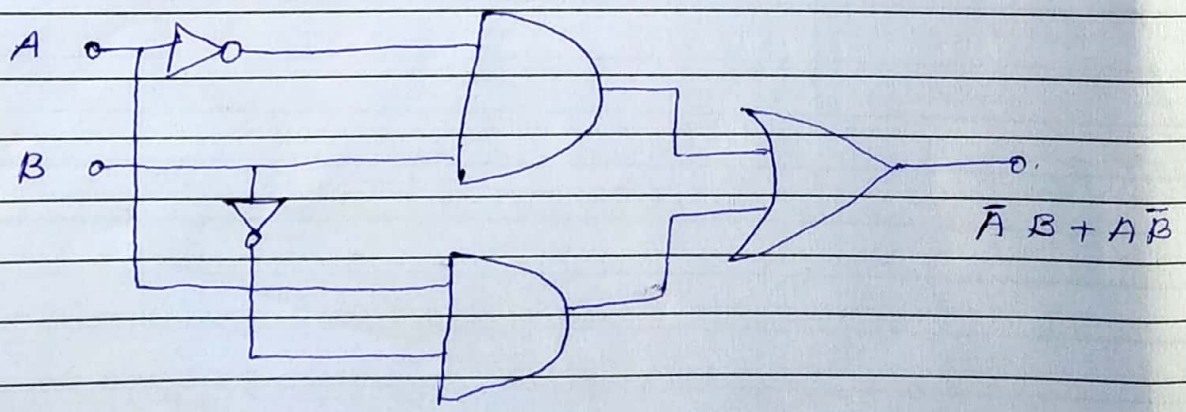
I/P A	I/P B	O/P	Minterms M
0	0	0	$M_0 = \bar{A}\,\bar{B}$
0	1	1	$M_1 = \bar{A}\,B$
1	0	1	$M_2 = A\,\bar{B}$
1	1	0	$M_3 = A\,B$

In minterms
0 = $\bar{A}$
1 = A

Σ and m are used to represent sum of miniterms

Expression of SOP is

$$F = \Sigma m(1, 2)$$
$$= \bar{A}B + A\bar{B}$$



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For three variable

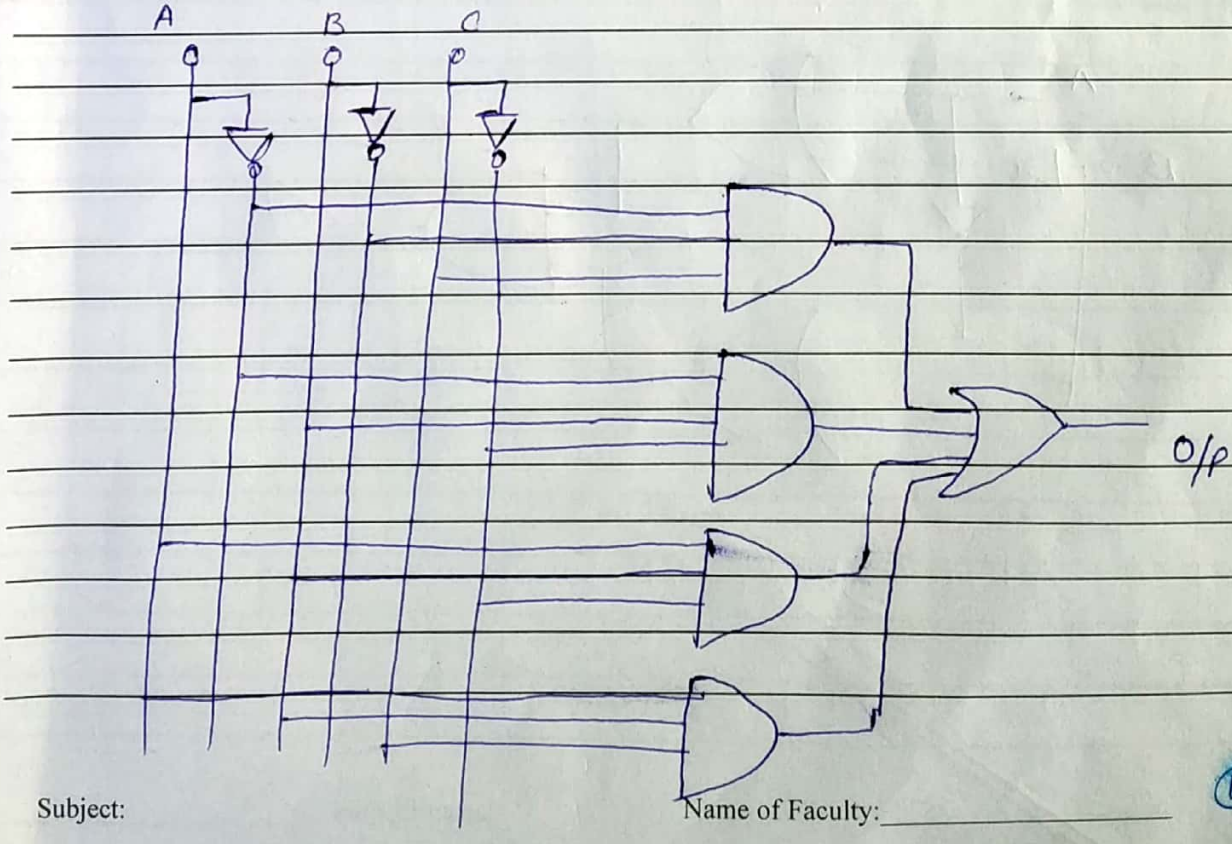
Truth table is

i/p			o/p	Minterms
A	B	C	o/p	m
0	0	0	0	$m_0 = \bar{A}\bar{B}\bar{C}$
0	0	1	1	$m_1 = \bar{A}\bar{B}C$
0	1	0	1	$m_2 = \bar{A}B\bar{C}$
0	1	1	0	$m_3 = \bar{A}BC$
1	0	0	0	$m_4 = A\bar{B}\bar{C}$
1	0	1	0	$m_5 = A\bar{B}C$
1	1	0	1	$m_6 = AB\bar{C}$
1	1	1	1	$m_7 = ABC$

Expression of SOP is

$$F = \Sigma m(1, 2, 6, 7)$$

$$= \bar{A}\bar{B}C + \bar{A}B\bar{C} + AB\bar{C} + ABC$$



POS = 0 = A
1 = $\bar{A}$

★ Product of Sum (POS) / Maxterms Representation (ΠM)

The expression of O/P is

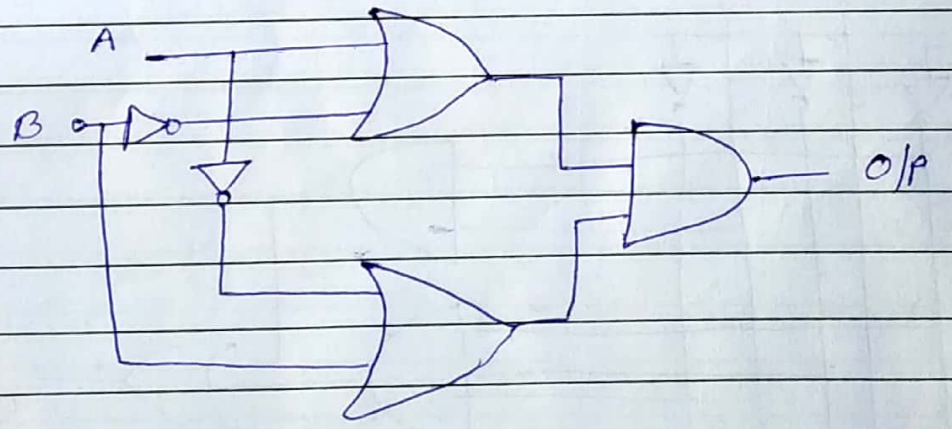
$F = (A + \bar{B})(\bar{A} + B)$

$= \Pi M(1, 2)$

$= (0\ 1)(1\ 0)$

Truth table

I/P A	I/P B	O/P	Maxterms
0	0	1	$M_0 = A + B$
0	1	0	$M_1 = A + \bar{B}$
1	0	0	$M_2 = \bar{A} + B$
1	1	1	$M_3 = \bar{A} + \bar{B}$



0 - $\bar{A}$
1 - A

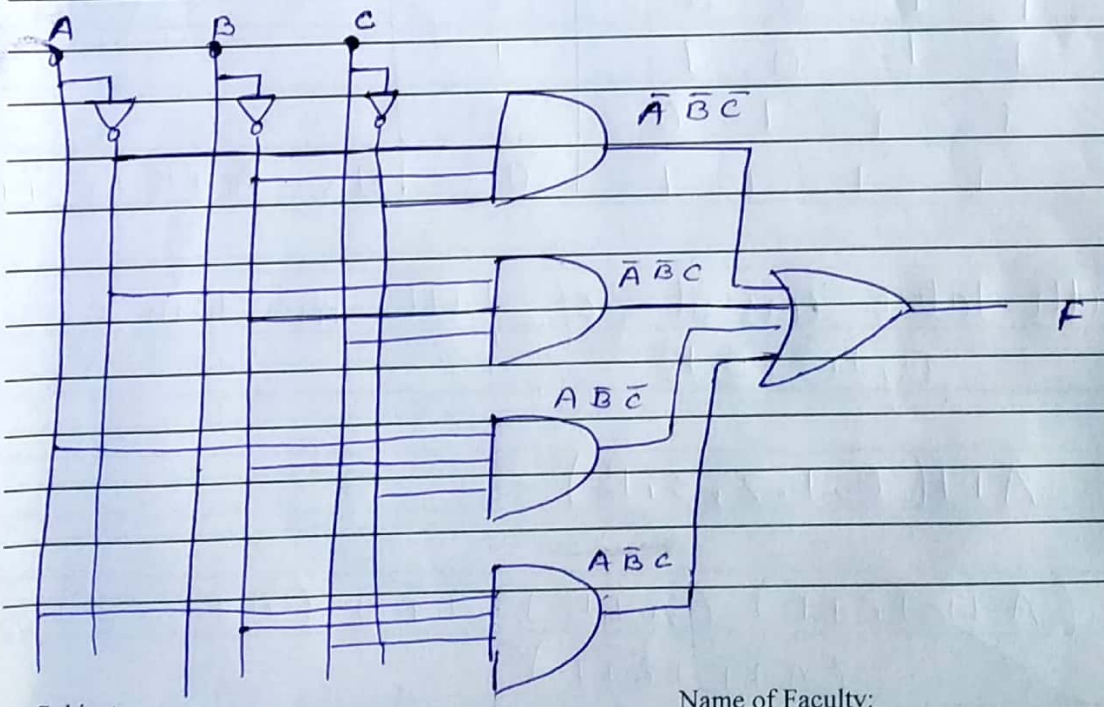
Q Determine boolean function of truth table shown below in terms of miniterms & draw logic dig

I/P A	I/P B	I/P C	O/P	Minterms ①
0	0	0	1	$M_0 = \bar{A}\bar{B}\bar{C}$
0	0	1	1	$M_1 = \bar{A}\bar{B}C$
0	1	0	0	$M_2 = \bar{A}B\bar{C}$
0	1	1	0	$M_3 = \bar{A}BC$
1	0	0	1	$M_4 = A\bar{B}\bar{C}$
1	0	1	1	$m_5 = A\bar{B}C$
1	1	0	0	$m_6 = AB\bar{C}$
1	1	1	0	$m_7 = ABC$

Expression of SOP is

$$F = \Sigma m(0,1,4,5)$$

$$= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C$$



Q Determine the boolean function of truth table in terms of maxterms & logic dig

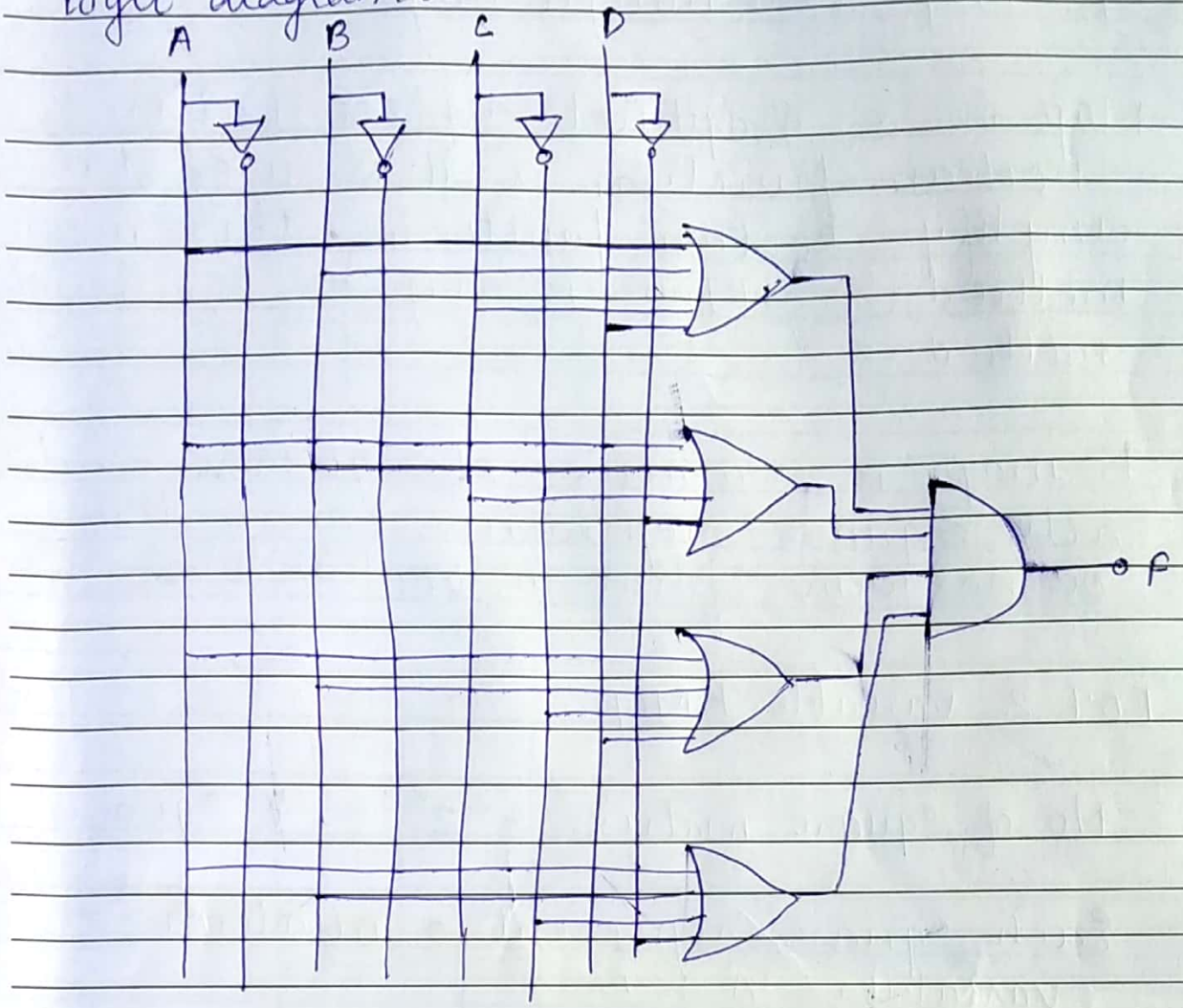
I/P 8 A	4 B	2 C	1 D	O/P O/P	Maxterms
0	0	0	0	0	$M_0 = A+B+C+D$
0	0	0	1	0	$M_1 = A+B+C+\bar{D}$
0	0	1	0	0	$M_2 = A+B+\bar{C}+D$
0	0	1	1	0	$M_3 = A+B+\bar{C}+\bar{D}$
0	1	0	0	1	
0	1	0	1	1	
0	1	1	0	1	
0	1	1	1	1	
1	0	0	0	1	
1	0	0	1	1	
1	0	1	0	1	
1	0	1	1	1	
1	1	0	0	1	
1	1	0	1	1	
1	1	1	0	1	
1	1	1	1	0	$M_{15} = \bar{A}+\bar{B}+\bar{C}+\bar{D}$

Truth table consist of full maxterm 0, 1, 2, 3, 15

$F = \Pi M(0, 1, 2, 3, 15)$

$= (A+B+C+D)(A+B+C+\bar{D})(A+B+\bar{C}+D)(A+B+\bar{C}+\bar{D})$.

Logic diagram is



H/W 1) Develop truth table for logic exp
$F = \Sigma m(1, 3, 5, 8, 7, 9, 12, 13)$

2) Develop truth table of logic exp
$F = \Pi M(0, 1, 2, 4, 5, 7)$

3) Develop truth table of logic exp
$F = \Sigma m(1, 2, 3, 4, 6, 7)$

4) Simplify the foll exp using boolean algebra
$F(A, B, C, D) = \Pi M(2, 4, 10, 12, 13, 14)$.

* K-Map (Karnaugh Map)

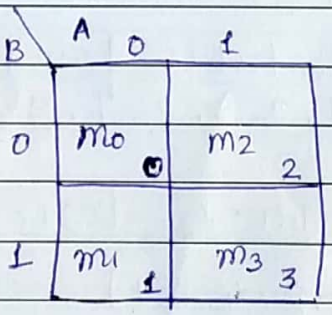
Map is a graphical representation of boolean function & it is used to simplify boolean function. This map method is klas K-map or Karnaugh method.

K-map is a matrix of squares and each square represents a minterms or maxterms form a boolean exp.

For 2 variable Kmap

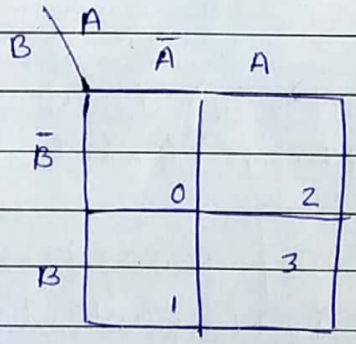
No of square matrix $= 2^2 = 4$ square

Each square represent a minterm in variables A & B.



$0 \rightarrow \bar{A}$

$1 \rightarrow A$



For 3 variable

$2^3 = 8$ = Square matrix.

C \ AB	00	01	11	10
0	0	2	6	4
1	1	3	7	5

$\bar{C}$ \ $A\bar{B}$	$\bar{A}\bar{B}$ 00	$\bar{A}B$ 01	AB 11	$A\bar{B}$ 10
0	0	2	6	4
1	1	3	7	5

For 4 variables

$2^4 = 16$ = Square matrix

CD \ AB	00	01	11	10
00	0	4	12	8
01	1	5	13	9
11	3	7	15	11
10	2	6	14	10

Q Truth table is shown below. find the expression & minterms & also draw K-map for it

i/p A	i/p B	o/p
0	0	0
0	1	1
1	0	1
1	1	1

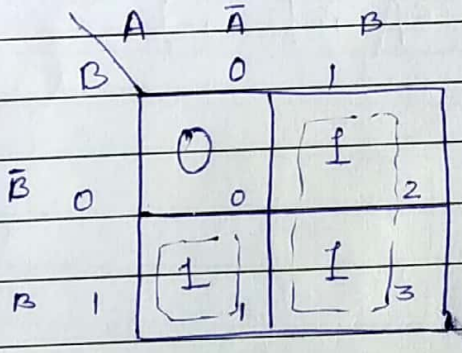
$0 \rightarrow \bar{A}$

$1 \rightarrow A$

=>

i/p A	i/p B	o/p	Minterms	Representation
0	0	0	$M_0 = \bar{A}\bar{B}$	0
0	1	1	$M_1 = \bar{A}B$	1
1	0	1	$M_2 = A\bar{B}$	2
1	1	1	$M_3 = AB$	3

K-Map



logic exp from K-map is

$F = B + \bar{A}B$

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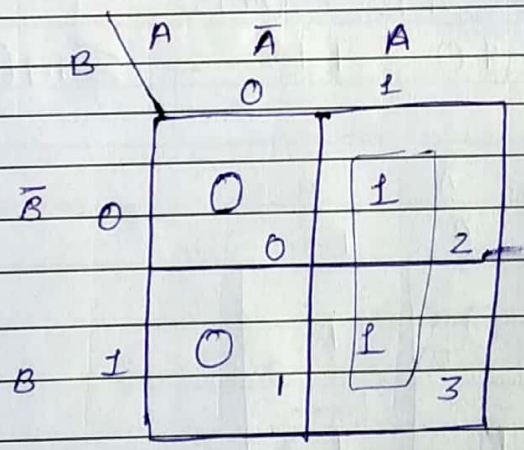
Q Truth table is shown below, write the boolean exp & also draw K-map.

I/P A	I/P B	O/P
0	0	0
0	1	0
1	0	1
1	1	1

=>

I/P A	I/P B	O/P	Minterms	Repres
0	0	0	$M_0 = \bar{A}\bar{B}$	0
0	1	0	$M_1 = \bar{A}B$	1
1	0	1	$M_2 = A\bar{B}$	2
1	1	1	$M_3 = AB$	3

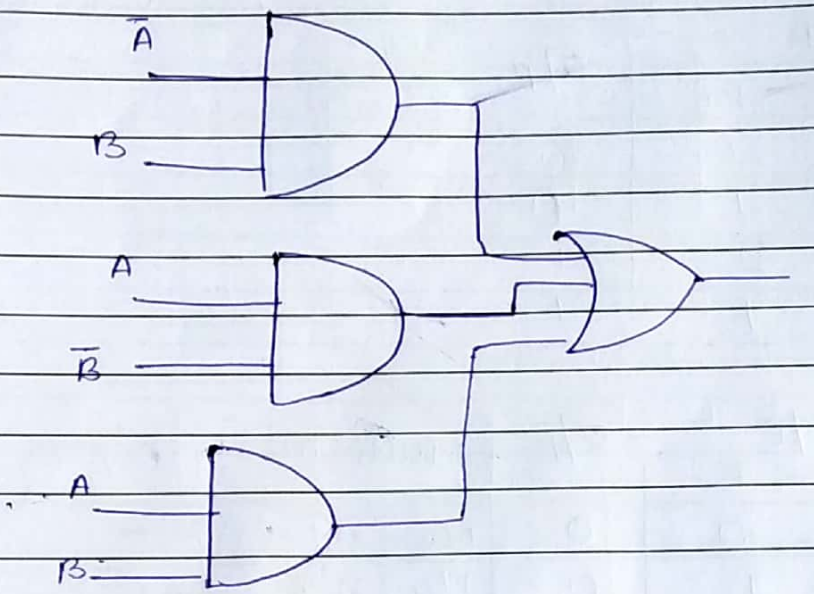
K-Map



Logic exp is

$F = A$

Q Simplify the logic dig, draw the K-map of it

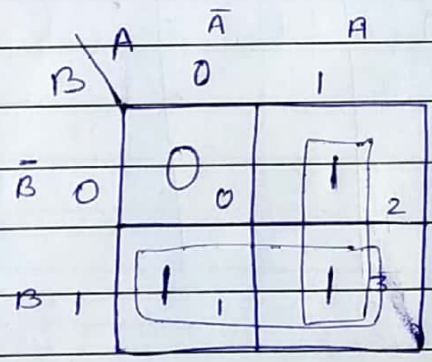


Logic exp is

$O/P = \bar{A}B + A\bar{B} + AB$

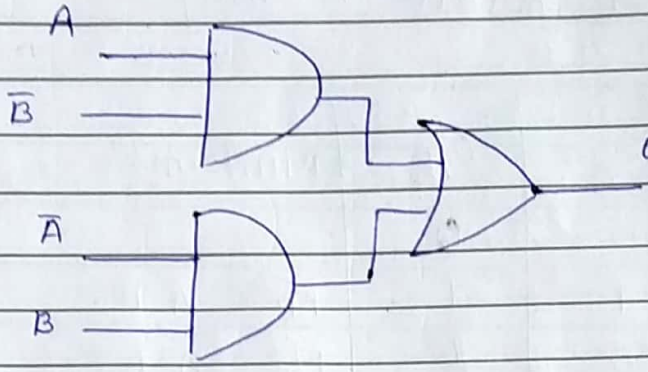
$= 01, 10, 11 = \Sigma m(1,2,3)$

K-map



K-map exp = A + B.

Q Simplify the logic dig & drive the exp & draw the K map



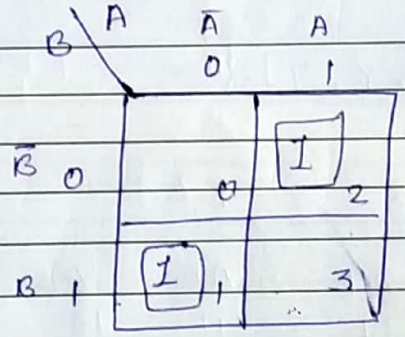
logic exp = $A\bar{B} + \bar{A}B$

= XY \ NQ

10 01

= $\Sigma m(1,2)$

K-map



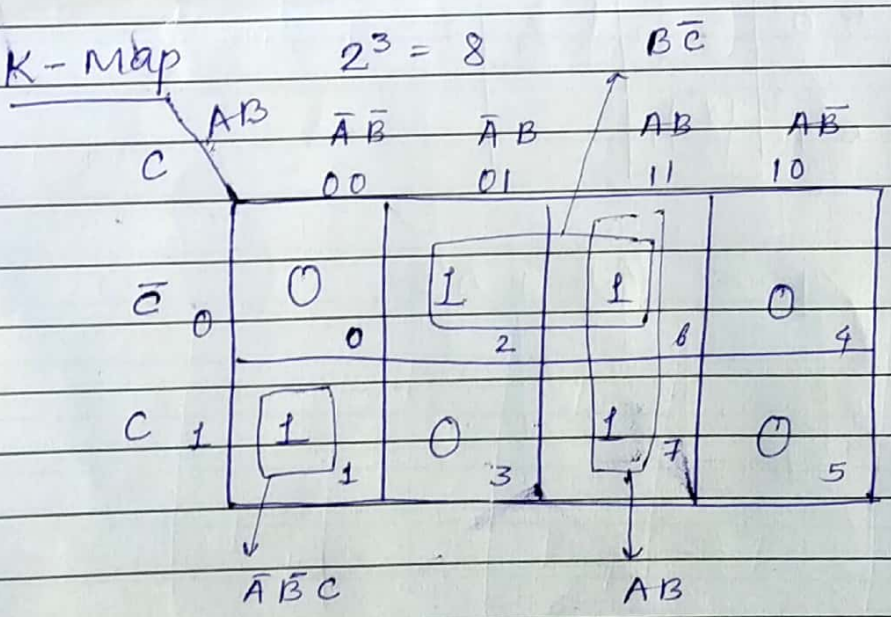
logic exp = $A\bar{B} + \bar{A}B$

Q: For the truth table shown below write boolean exp in terms of minterms and also draw K-map

I/P			O/P	Minterms
A	B	C		
0	0	0	0	
0	0	1	1	$M_1 = \bar{A}\bar{B}C$
0	1	0	1	$M_2 = \bar{A}B\bar{C}$
0	1	1	0	
1	0	0	0	
1	0	1	0	
1	1	0	1	$M_6 = AB\bar{C}$
1	1	1	1	$M_7 = ABC$

$F = \Sigma m(1, 2, 6, 7)$.

K-Map $2^3 = 8$



logic exp = $AB + \bar{A}\bar{B}C + B\bar{C}$

Q Construct a K-map for boolean function

$$O = AB + C\bar{D}$$

⇒ expression is $O = AB + C\bar{D}$ is four variable so K-map consists of $2^4 = 16$ squares.

CD \ AB	$A\bar{B}$ 00	$\bar{A}B$ 01	AB 11	$A\bar{B}$ 10
$\bar{C}\bar{D}$ 00	0	4	1 12	8
$\bar{C}D$ 01	1	5	1 13	9
CD 11	3	7	1 15	11
$C\bar{D}$ 10	1 2	1 6	1 14	1 10

Q Consider the expression & draw the K-map.

$$\bar{A}B + A\bar{B} + AB$$

⇒ Logic exp = $\bar{A}B + A\bar{B} + AB$

= 01 10 11

= $\Sigma m(1, 2, 3)$

K-map

B \ A	$\bar{A}$ 0	A 1
$\bar{B}$ 0	0	1 2
B 1	1 1	1 3

H/w : 1) Consider the exp & draw the K-map

a) $\Sigma m\ (0,2,3)$

b) $\bar{A}B + A\bar{B}$

c) $\bar{A}\bar{B} + A\bar{B} + AB$

d) $\bar{A}\bar{B} + \bar{A}B + AB$

e) $A\bar{B}C + \bar{A}BC$

Q Consider the exp and draw K-map

$$\bar{A}\bar{B}C + A\bar{B}C + \bar{A}B\bar{C} + AB\bar{C} + ABC$$

⇒ logic exp is

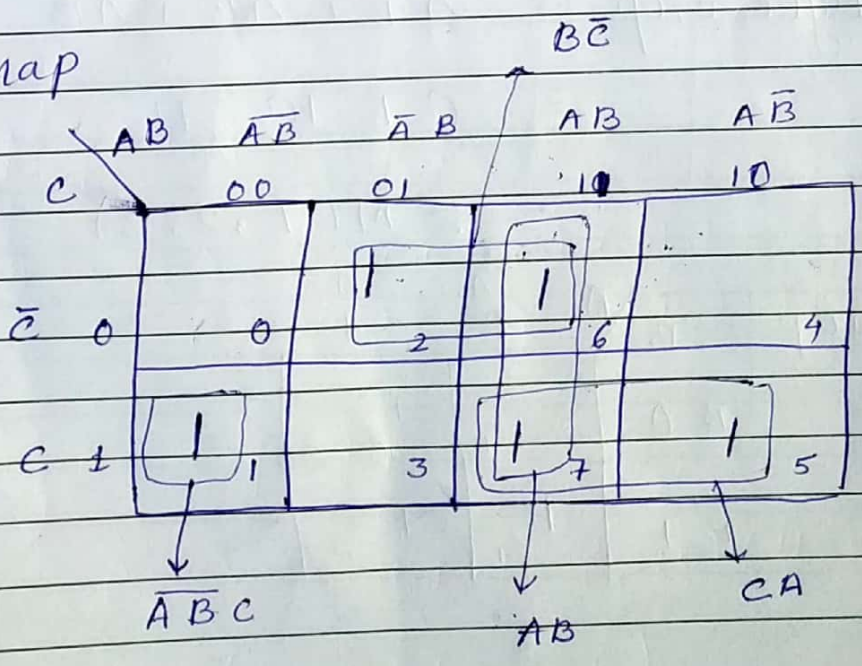
$$\bar{A}\bar{B}C + A\bar{B}C + \bar{A}B\bar{C} + AB\bar{C} + ABC$$

001 101 010 110 111

$= \Sigma m(1,5,2,6,7)$

$2^3 = 8$

K-Map



Subject: logic exp = $AB + AC + B\bar{C} + A\bar{B}C$

Name of Faculty:

Q Plot the exp on K-map.

$Y = AB\bar{C} + ABC + \bar{A}\bar{B}C$.

$Y = \bar{A}\bar{B}C + \bar{A}BC$

$Y = \bar{A}BC + ABC$

$Y = \bar{A}BC + ABC$.

$Y = A\bar{B}\bar{C} + AB\bar{C}$

$0 \rightarrow A$
$1 \rightarrow \bar{A}$

Q plot the expression $(A+B)(\bar{A}+B)(\bar{A}+\bar{B})$ on K-map.

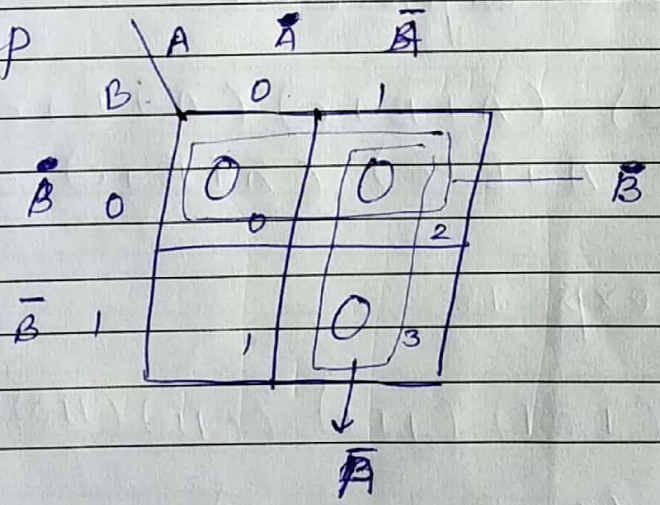
⇒ Logic exp is

$(A+B)(\bar{A}+B)(\bar{A}+\bar{B})$

0 0 1 0 1 1

$= \pi M(0, 2, 3)$.

K-map

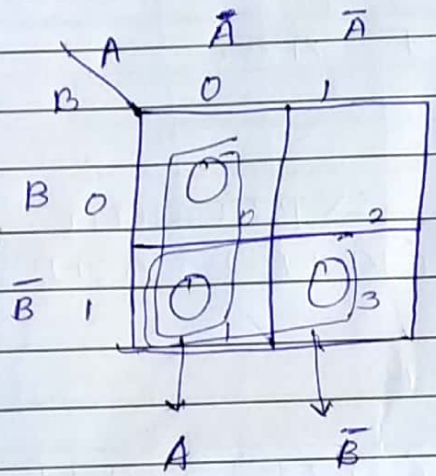


Q Reduce the expression
$(A+B)(A+\bar{B})(\bar{A}+\bar{B})$ using mapping

=> logic exp is
$(A+B)$ $(A+\bar{B})$ $(\bar{A}+\bar{B})$
0 0 0 1 1 1

$= \Pi M(0,1,3)$

K-map



0 $\frac{A}{\bar{A}}$ 1

logic exp is $A+\bar{B}$

Q Map the expression

$(A+B+C)$ $(\bar{A}+B+\bar{C})$ $(\bar{A}+\bar{B}+\bar{C})$
$(A+\bar{B}+\bar{C})$ $(\bar{A}+\bar{B}+C)$

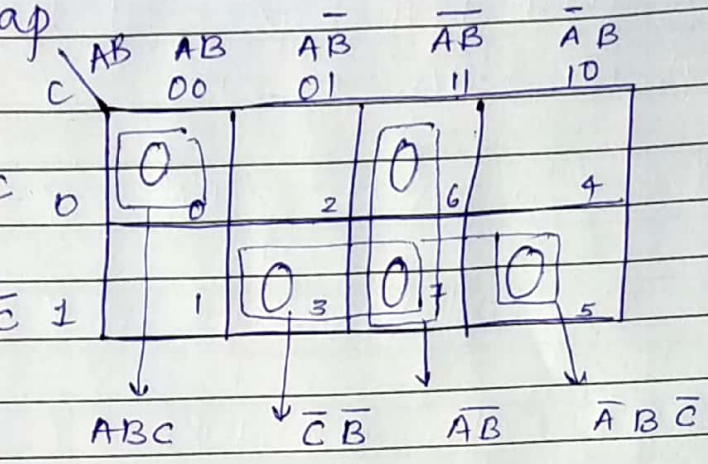
=> logic exp is

(000) (101) (111) (011) (110)
4 2 1

$= \Pi M(0,5,7,3,6)$

Subject: Name of Faculty:

K-Map



logic exp = $ABC + \bar{B}\bar{C} + A\bar{B} + \bar{A}B\bar{C}$

Q: Plot the boolean exp on K-map

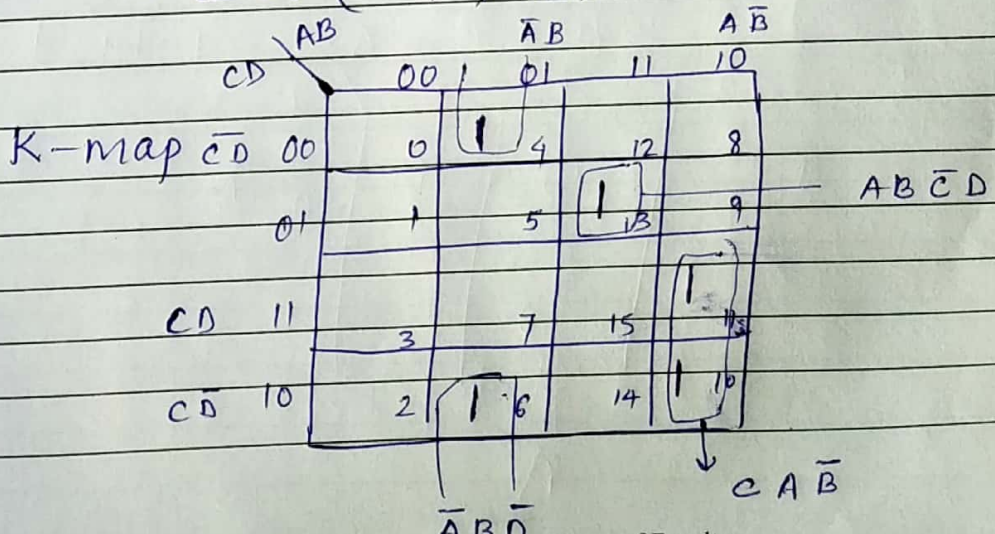
0 - $\bar{A}$
1 - A

$Y = \bar{A}B\bar{C}\bar{D} + A\bar{B}C\bar{D} + AB\bar{C}D + \bar{A}BC\bar{D} + A\bar{B}CD$

$\Rightarrow$

logic expn = $\overset{8\ 4\ 2\ 1}{(0100)}\ (1010)\ (1101)\ (0110)\ (1011)$

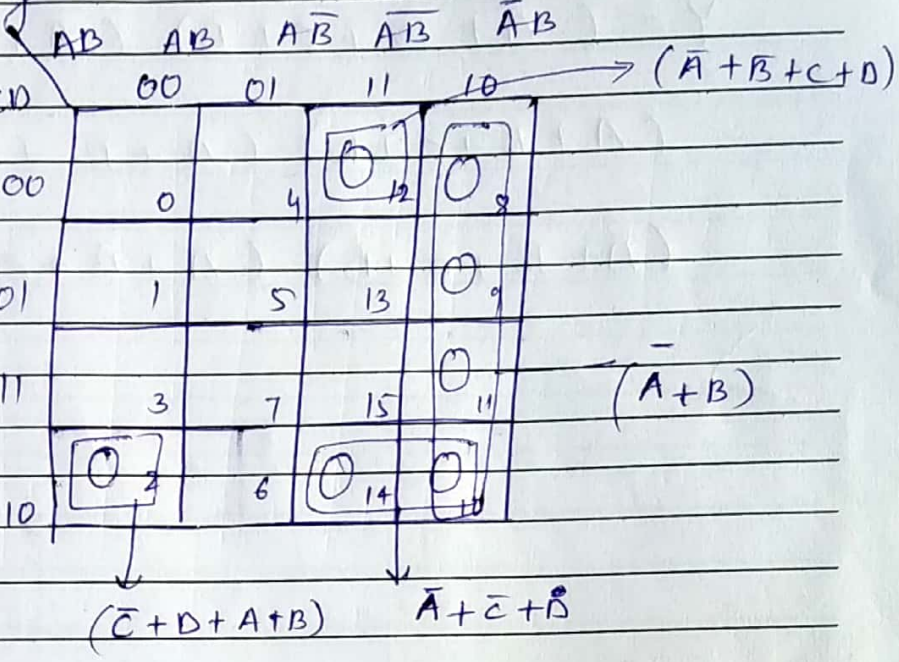
$= \Sigma M\ (4, 10, 13, 6, 11)$



Q Reduce the foll expression

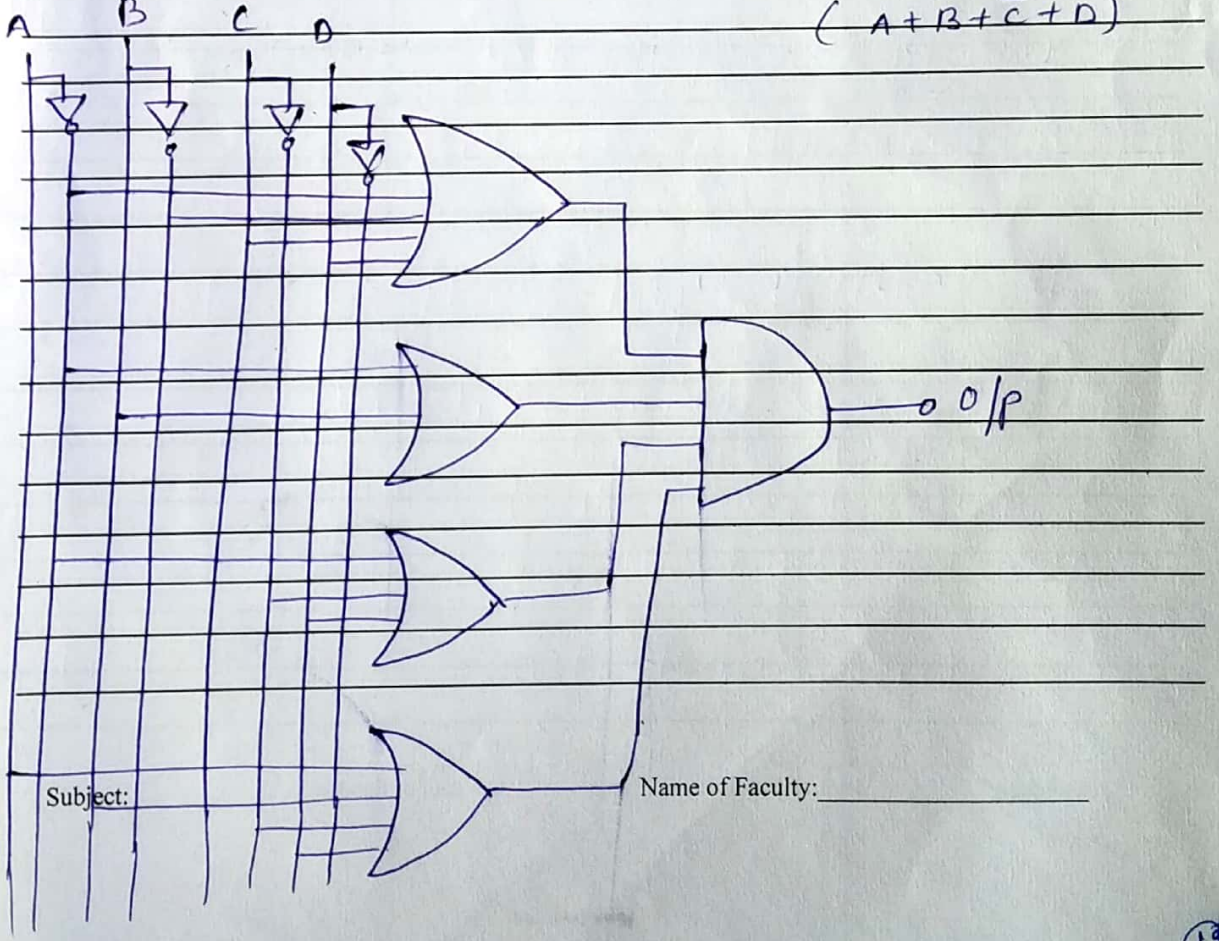
$\Pi m(2, 8, 9, 10, 11, 12, 14)$ & implement it using gates.

K-map



logic exp = $(\bar{A}+\bar{B}+C+D) \cdot (\bar{A}+B) \cdot (\bar{A}+\bar{C}+D)$

$(A+B+\bar{C}+D)$



Q Minimize the following expression in POS form

$Y = (\bar{A} + \bar{B} + C + D)(\bar{A} + \bar{B} + \bar{C} + D)$

$(A + B + C + D)(A + \bar{B} + \bar{C} + D)(A + \bar{B} + \bar{C} + \bar{D})$

$(\bar{A} + \bar{B} + C + \bar{D})(\bar{A} + \bar{B} + \bar{C} + \bar{D})(\bar{A} + B + C + D)$.

Q $Y = \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}D$ is the logic expression. Draw the K-map.

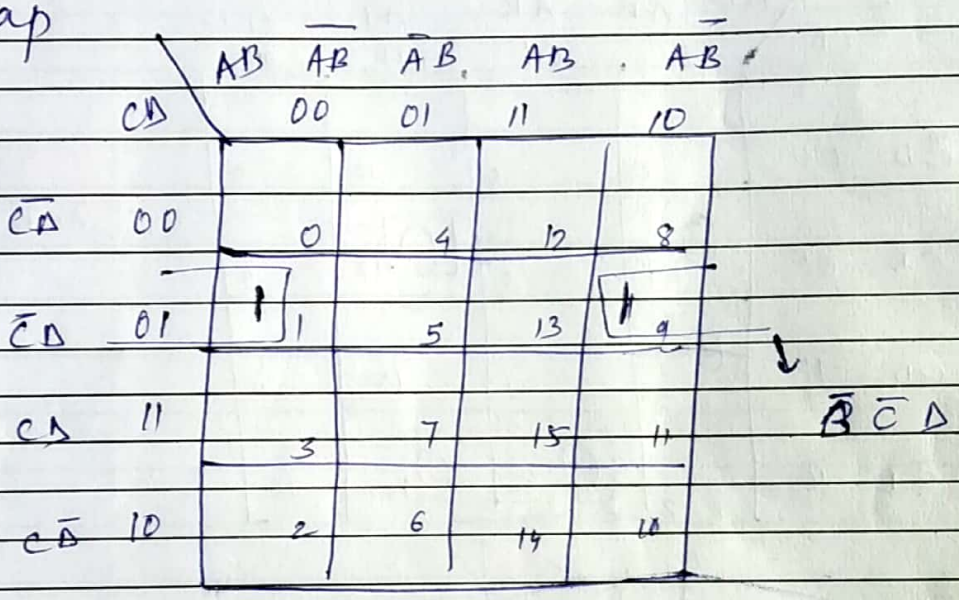
⇒

$Y = \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}D$

$= 0001 \quad 1001$

$= \Sigma M(1, 9)$

K-Map



Logic exp is $Y = \bar{B}\bar{C}D$.

Q 8

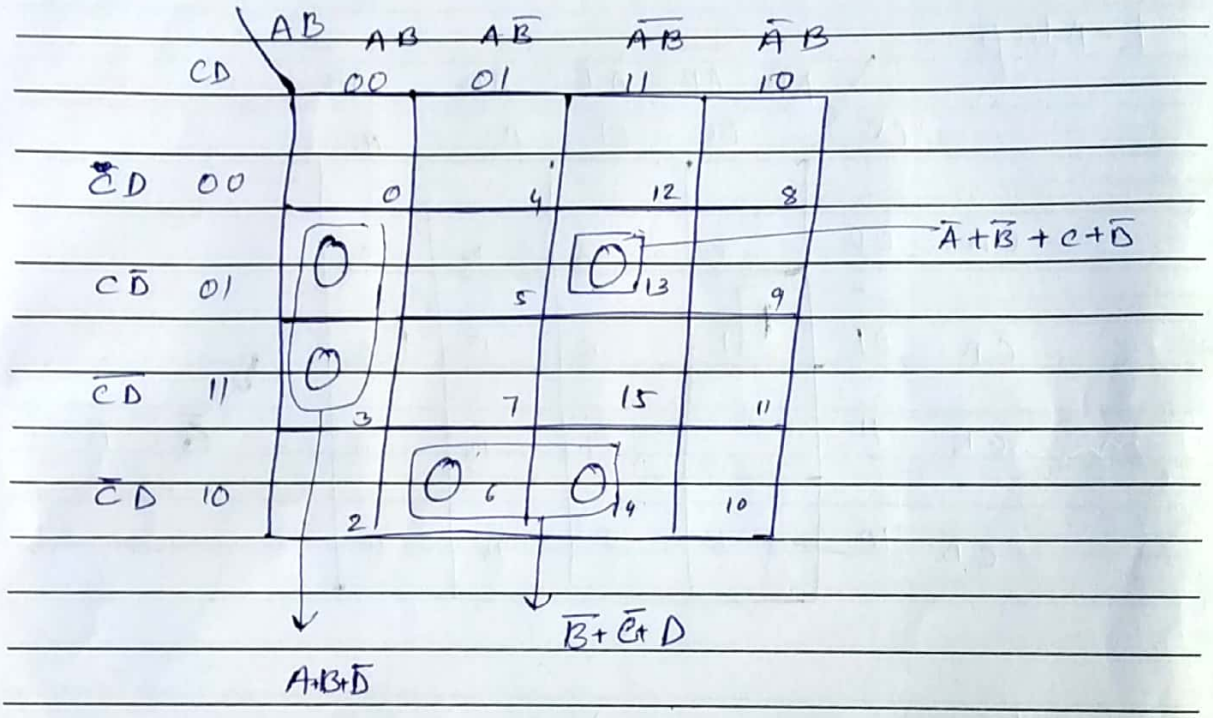
Q Plot the boolean exp

$Y = (A+B+C+\bar{D})\ (A+\bar{B}+\bar{C}+D)\ (A+B+\bar{C}+\bar{D})\ (\bar{A}+\bar{B}+C+\bar{D})\ (\bar{A}+\bar{B}+\bar{C}+D)$

POS 0 - A
1 - $\bar{A}$

$\Rightarrow Y = \bar{\Pi} M\ (1, 6, 3, 13, 14)$.

(8 4 2 1)
(0 0 0 1) (0 1 1 0) (0 0 1 1) (1 1 0 1) (1 1 1 0)



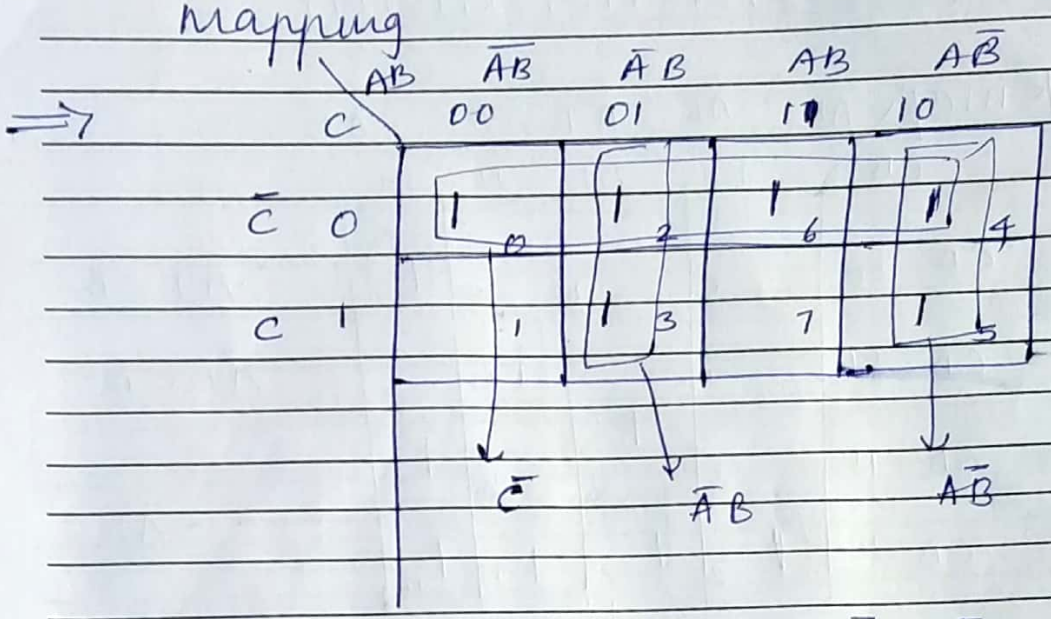
logic exp is = $(A+B+\bar{D}) \cdot (\bar{B}+\bar{C}+D) \cdot (\bar{A}+\bar{B}+C+\bar{D})$.

Q Plot the boolean Algebra

$Y = (A+\bar{B}+C)\ (A+\bar{B}+\bar{C})\ (\bar{A}+\bar{B}+C)\ (A+B+\bar{C})$

Q Reduce the expression $\Sigma m(0,2,3,4,5,6)$ using mapping

$2^3=8$



logic exp is $Y = \bar{A}B + A\bar{B} + \bar{C}$

HW

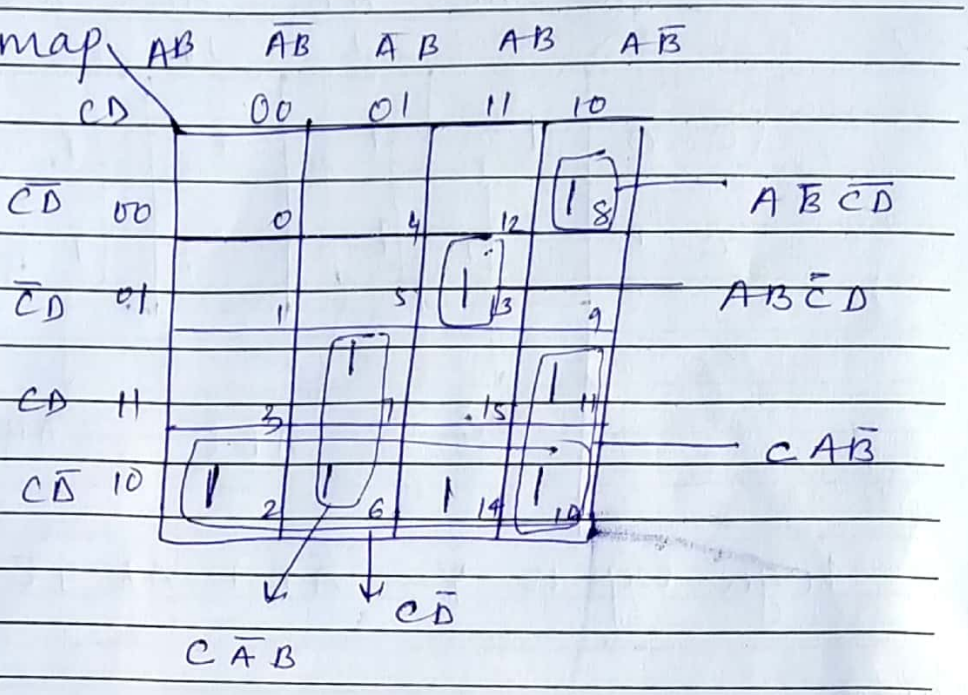
Q Reduce the expression $\Sigma m[0,1,2,3,4,7]$ using mapping

Q Reduce the expression $\Sigma m(1,2,4,6,7)$ using mapping & implement it using gates

Q Reduce using mapping the expression

$\Sigma m\,(2,3,6,7,8,10,11,13,14)$

⇒ Kmap



logic exp = $A\bar{B}\bar{C}\bar{D} + AB\bar{C}D + A\bar{B}C + C\bar{D} + \bar{A}BC$.

Q Reduce the exp using & implement it using logic gate

$\Sigma m(0,1,2,3,5,7,8,9,10,12,13)$

Q Reduce the foll function using k-map

$f(A,B,C,D) = \Sigma m\,(0,1,4,8,9,10)$

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(*) Don't Care Combination

As O/P of function is dependent on I/P variables. But in some cases O/P does not matter on combination of I/P variables

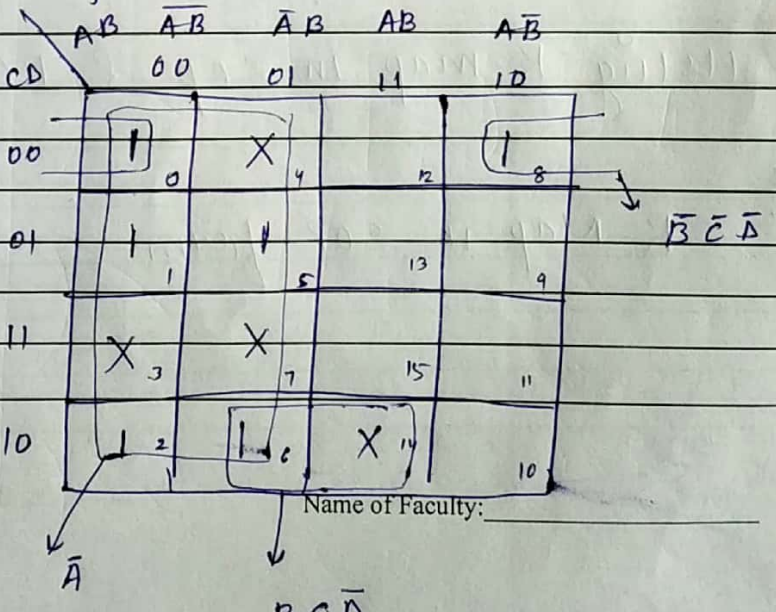
This happened as I/P combination are invalid & O/P corresponding to these I/P combination have no importance. These type of I/P combination are c/as don't care & are indicated by x & that can be either 0 or 1

Either 0 or 1 is used in place of x so as to make the expression in the simplest form.

Q Simplify the logic function

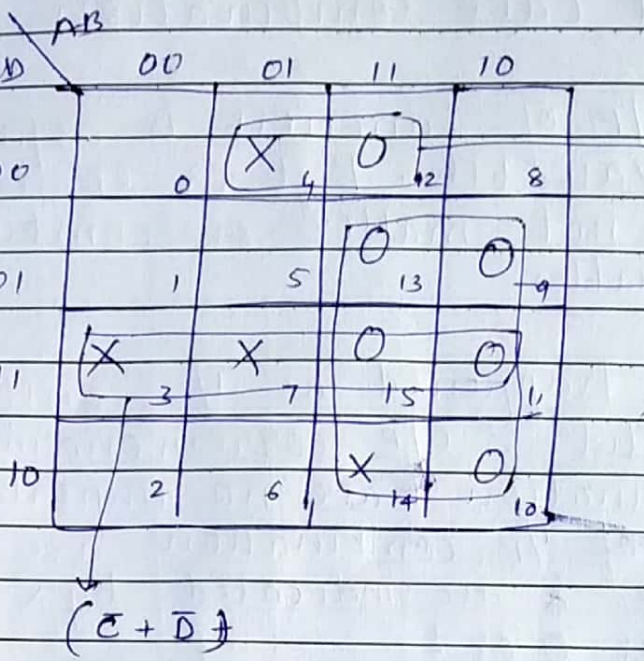
$f(A,B,C,D) = \Sigma m(0,1,2,5,6,8) + d(3,4,7,14)$ using k-map in SOP & POS

In SOP



$f(A, B, C, D) = \bar{A} + \bar{B}\bar{C}\bar{D} + BC\bar{D}$

9n POS



logic exp $f(A, B, C, D) = (\bar{B}+C+D)(\bar{A}+\bar{C}+\bar{D})(\bar{C}+\bar{D})$

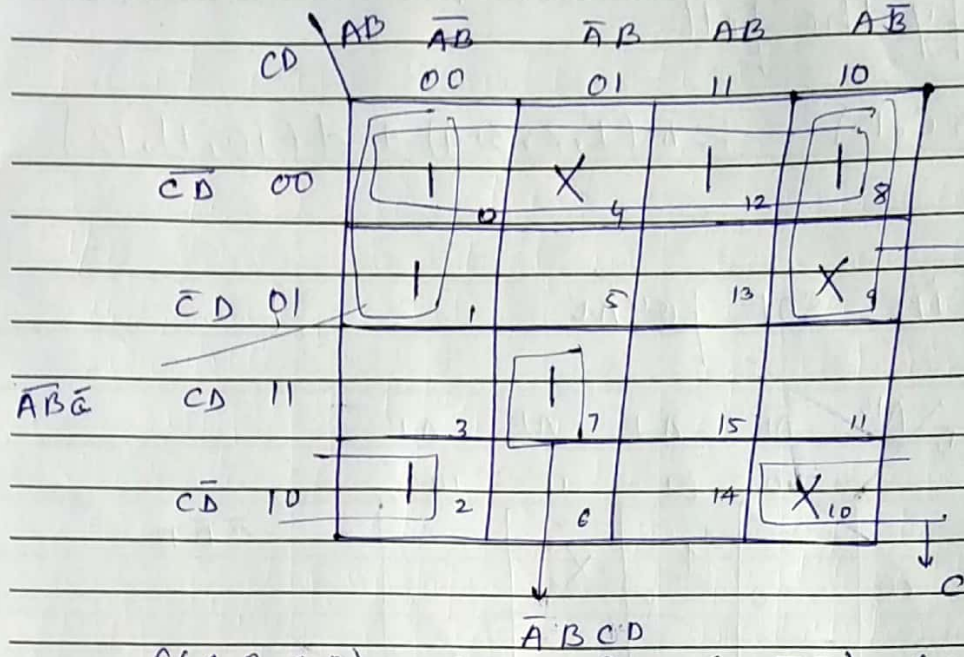
Q Simplify the logic expression

$f(A, B, C, D) = \pi(3, 5, 6, 11, 13, 14, 15) + d(4, 9, 10)$

Using K-map in SOP & POS form.

Ans

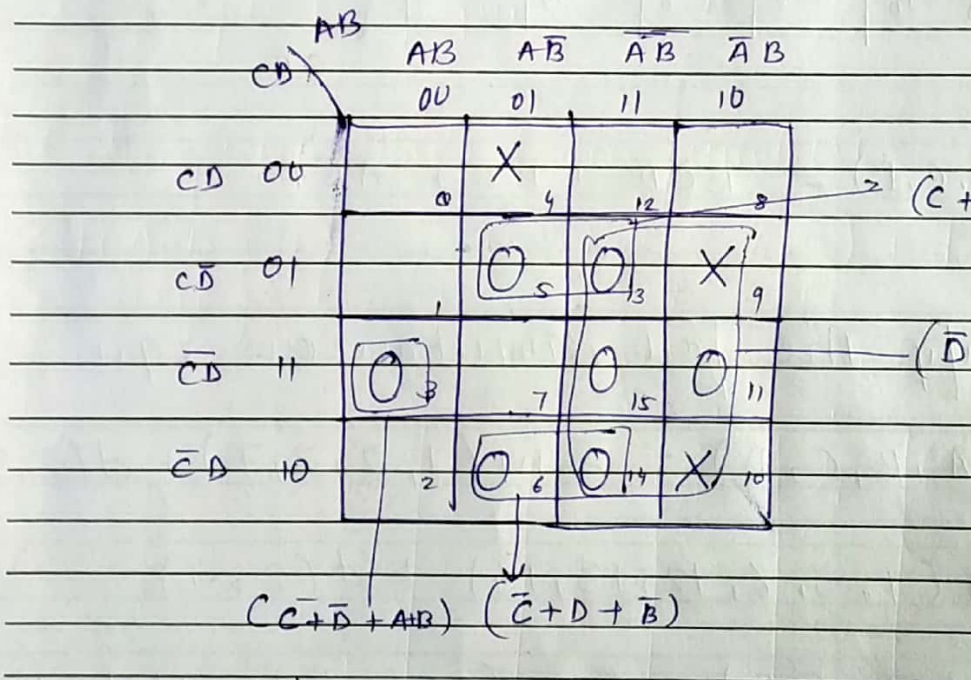
K-Map in SOP form



$f(A,B,C,D) = (\bar{A}BCD) + (C\bar{D}\bar{B}) + (A\bar{B}\bar{C}) + (\overline{A}BC)$

In

POS form



$f(A,B,C,D) = (C+\bar{D}+\bar{B})(\bar{D}+\bar{C})(\bar{C}+D+\bar{B})(\bar{C}+\bar{D}+A+B)$.

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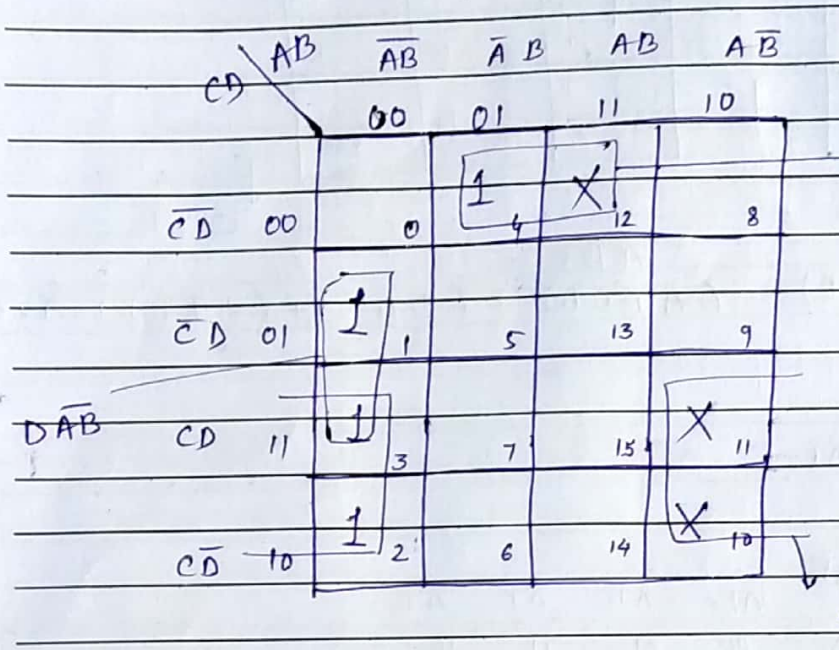
Q Simplify the fall

$f(A, B, C, D) = \Sigma m(1,2,3,4) + d(10,11,12)$

K-Map in SOP form



$f(A, B, C, D) = B\bar{C}\bar{D} + \bar{B}C + \bar{A}\bar{B}D$

Q Simplify the fall simultaneous eqn

1) $f(A, B, C, D) = \Sigma m(1, 2, 3, 7) + d(8, 9, 10)$

2) $\Sigma m(1, 5, 6, 12, 13, 14) + d(2, 4)$

3) $f(A, B, C, D) = \Sigma m(0, 2, 6, 10, 11, 12, 13) + d(3, 4, 5, 14, 15)$

Q $f_2 = \Sigma m(1,2,6,7,8,13,14,15) + d(3,5,12)$

Q $f_1(x_1 x_2 x_3 x_4) = d(12,14) + \Sigma m(1,2,3,5,7,8,9)$.

Q $f_2(x_1 x_2 x_3 x_4) = d(10,11) + \Sigma m(0,1,2,3,4,6,8,9)$

Q $f_2(x_1 x_2 x_3 x_4) = d(14,15) + \Sigma m(1,3,5,7,8,9,12,13)$.

Q Reduce the foll function using Karnaugh map technique

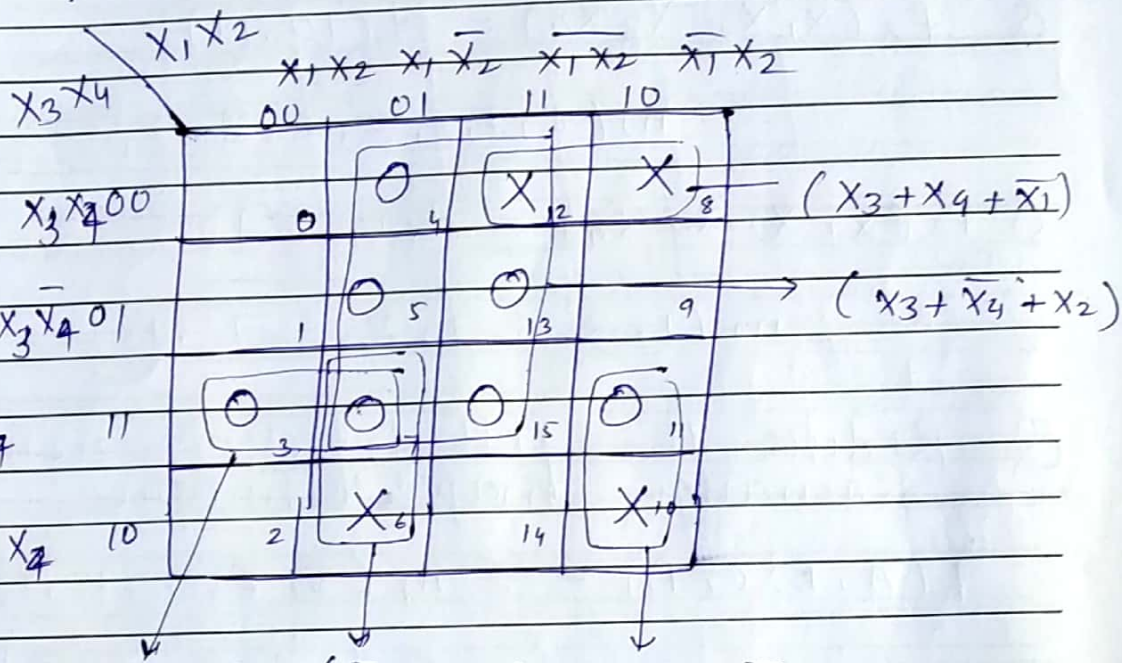
$f(A,B,C,D) = \Sigma m(5,6,7,12,13) + \Sigma d(4,9,14,15)$.

Q Simplify using K-Map

$f(X_1 X_2 X_3 X_4) = \Pi m(3,4,5,7,11,13,15) \cdot d(6,8,10,12)$

$\Rightarrow$

K-Map in POS form



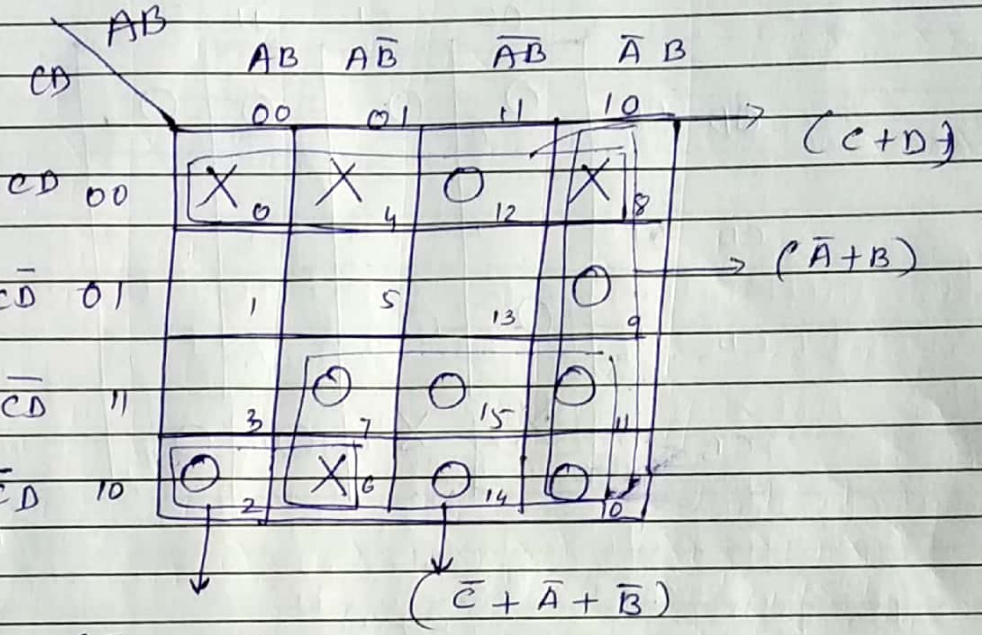
$f(X_1 X_2 X_3 X_4) = (X_3+X_4+\bar{X}_1) \cdot (X_3+\bar{X}_4+X_2)$

$\cdot (\bar{X}_3+\bar{X}_4+X_1)(\bar{X}_3+X_1+\bar{X}_2)(\bar{X}_3+\bar{X}_1+X_2)$

Q) Simplify boolean expression using K-map

$f(A,B,C,D) = \Pi m(2,7,9,10,11,12,14,15) \cdot d(0,4,6,8)$

⇒ K-map in POS form



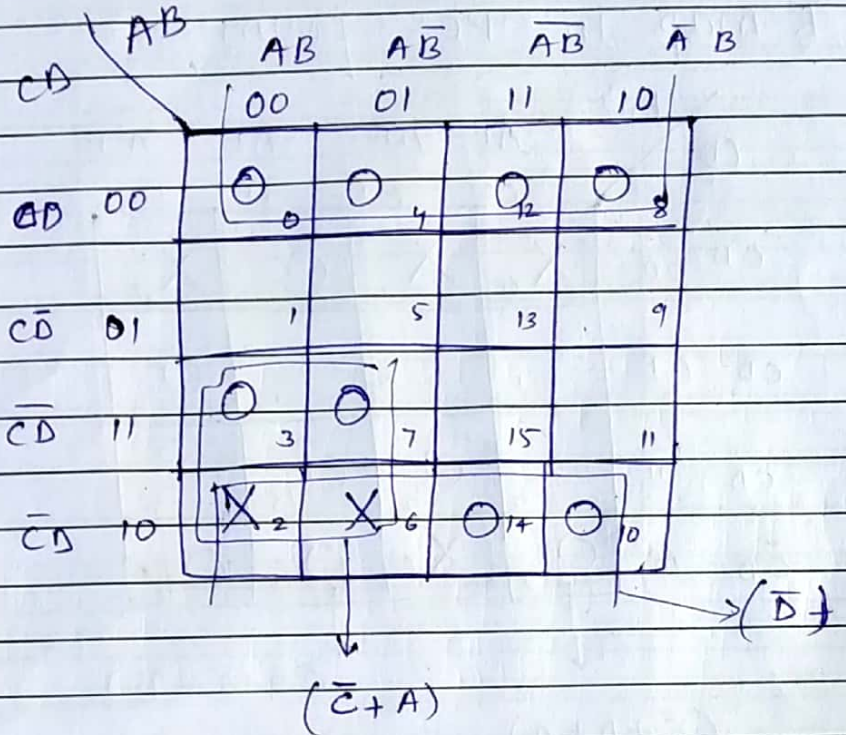
$f(A,B,C,D) = (C+D)\cdot(\bar{A}+B)(\bar{A}+\bar{B}+\bar{C})\cdot(A+\bar{C}+D)$

Q Simplify using K-Map

$f(A,B,C,D) = d(2,6) + \Pi m(0,3,4,7,8,10,12,14)$

⇒

K-map in POS form



$f(A,B,C,D) = \bar{D} \cdot (A+\bar{C})$.

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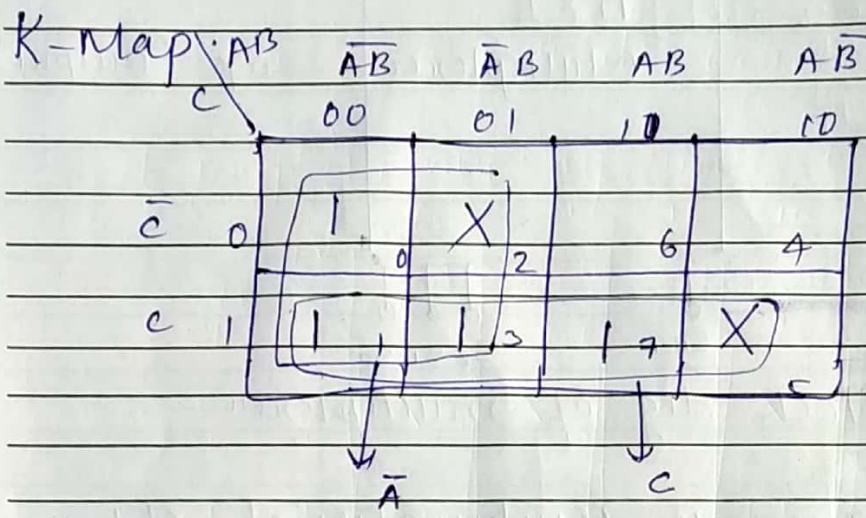
Q Implement the foll function

$$F(A,B,C) = \Sigma m\,(0,1,3,7) + \Sigma d(2,5)$$

K-Map:



$$F(A,B,C) = \bar{A} + C$$

Q Find the reduced SOP form of the foll function

$$F(W,X,Y,Z) = \Sigma d(2,5,13) + \Sigma m\,(0,7,8,9,10,12)$$

⭐ Multiplexer (MUX).

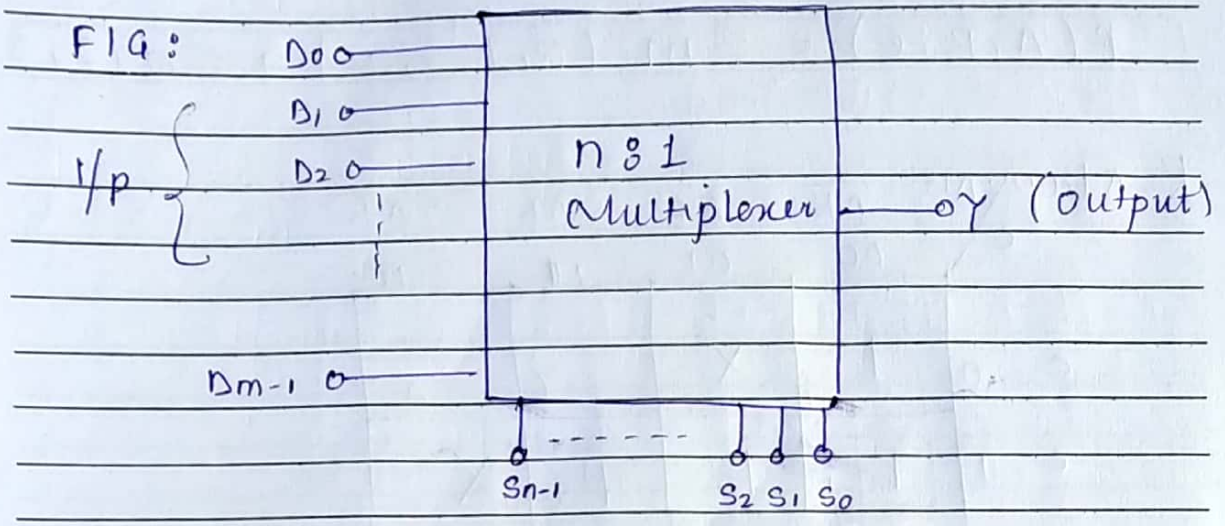


Fig: Block dig of multiplexer

1) The multiplexer is combinational ckt widely used standard ckt in digital design
2) The mux or data selector is a logic ckt that gets one out of several input to a single o/p.
3) The input selected is controlled by a set of select i/p above fig shows the block dig of mux with n i/p lines & one o/p lines
4) Selecting one out of n i/p for connection to the o/p. A set of m select i/p is required where

$$2^m = n$$

5) Depending on the digital code applied at the select i/p, one out of n data i/p is selected and transmitted to the single o/p Y.

6) Mux acts like digitally controlled multi position switch. The digital code applied to the select i/p determines which data i/p will be switched to the o/p

Application:

1) Data acquisition system

2) Reduce no of wire required to transfer data from source to destination

3) to simplify logic design

Various types of MUX are

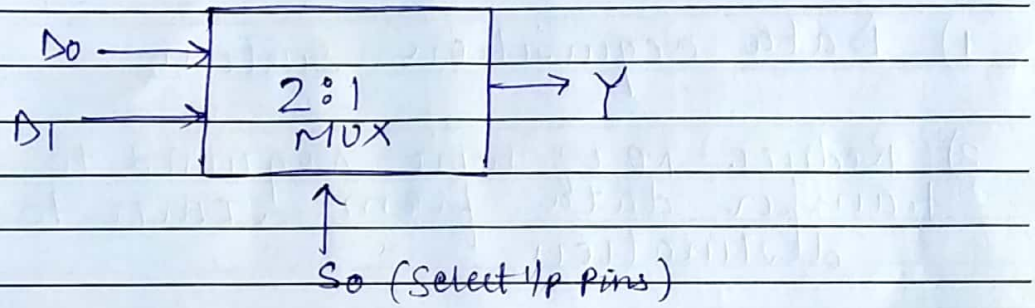
1) 2:1
2) 4:1
3) 8:1 etc.

1> 2:1 Multiplexer

$2^m = n$

if $m = 1$ = no of select pins

$2^1 = 2$ = Input



logic digram:

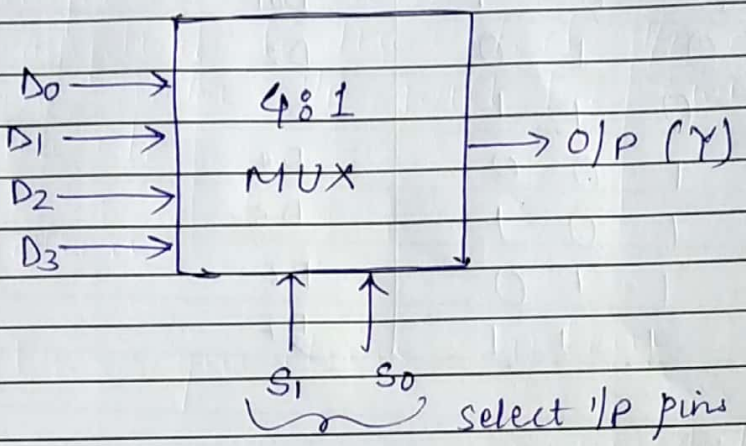
	S0	O/P
$\bar{S}_0$	0	D_0
S_1	1	D_1

2) 4:1 Multiplexer.

$2^m = n$

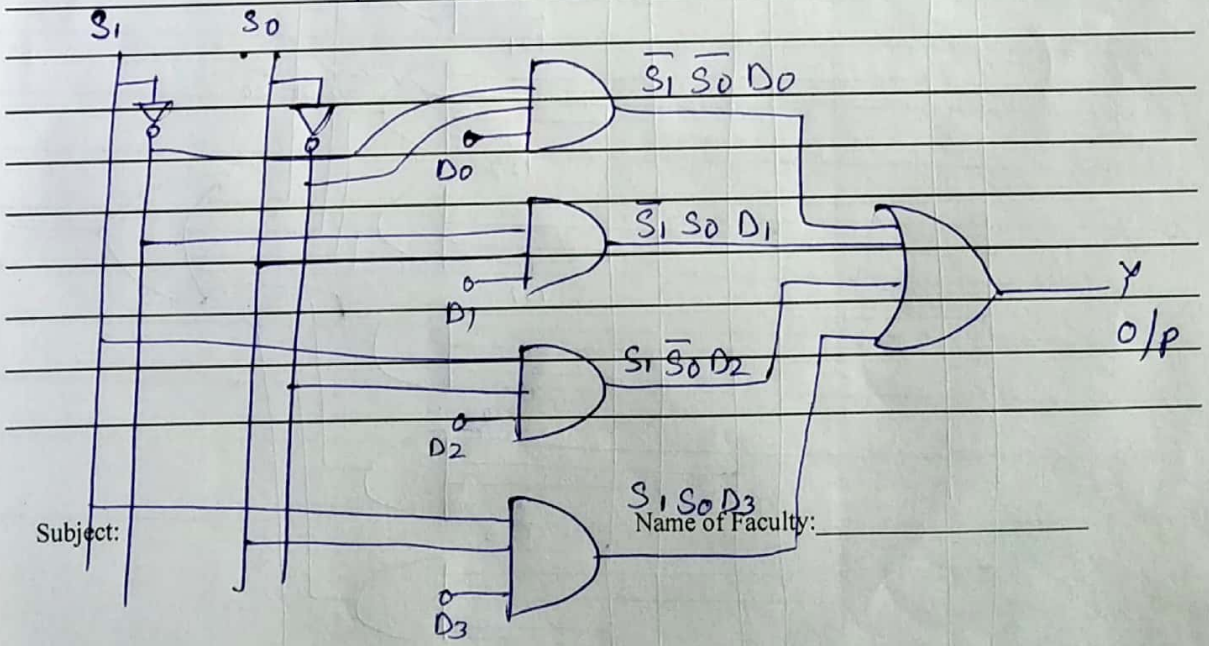
$2^2 = 2^m = 4. =$ no of i/p

$m = 2 =$ no of select pins



logic dig

S_1	S_0	Y (O/P)
$\bar{S_1}$ 0	0 $\bar{S_0}$	D0
$\bar{S_1}$ 0	1 S_0	D1
S_1 1	0 $\bar{S_0}$	D2
S_1 1	1 S_0	D3.



Subject: Name of Faculty: _____

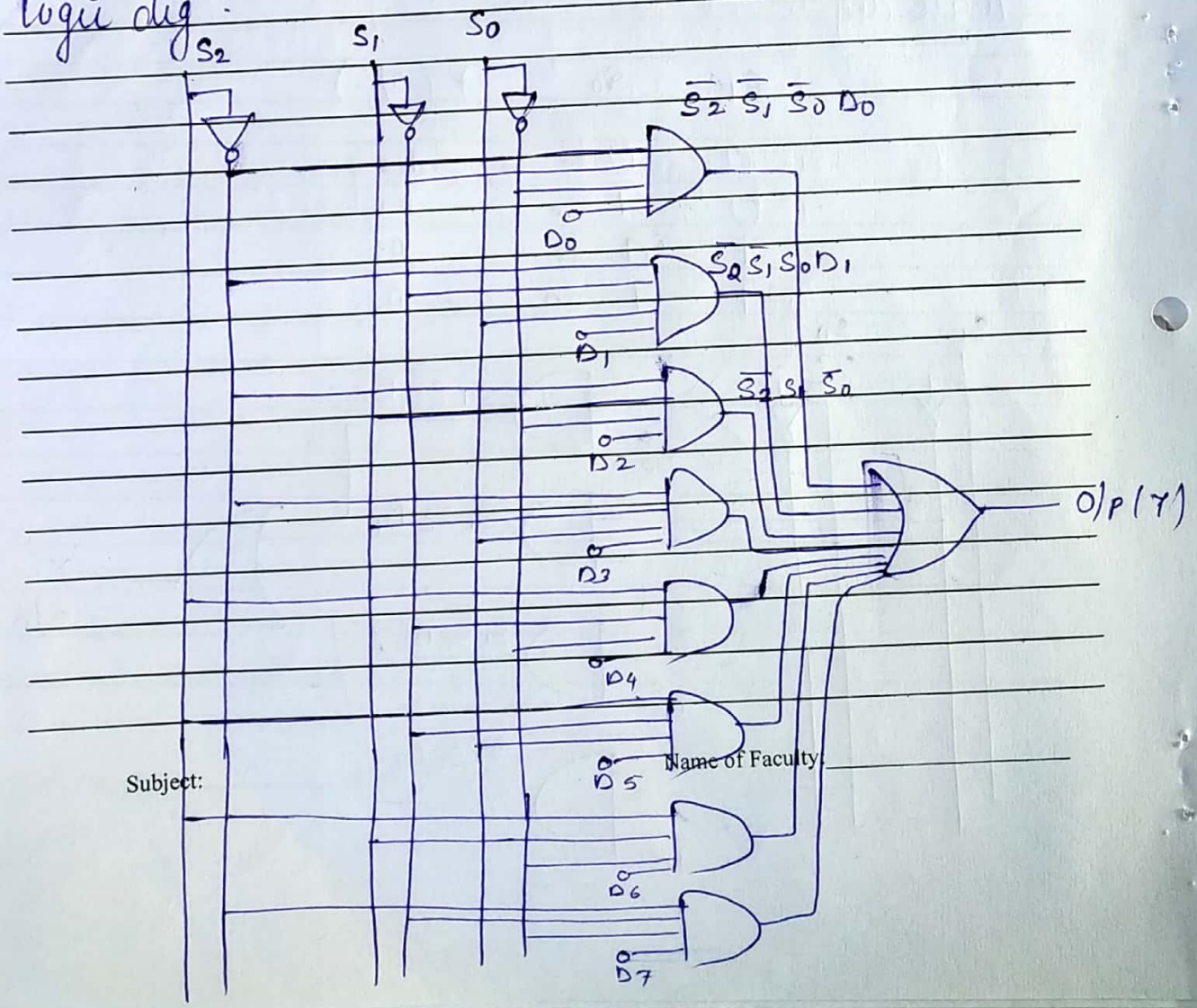
3) 8:1 MUX $2^m = 2^3 = 8$ = No of I/P

$m = 3$ = Select Pins

Truth table

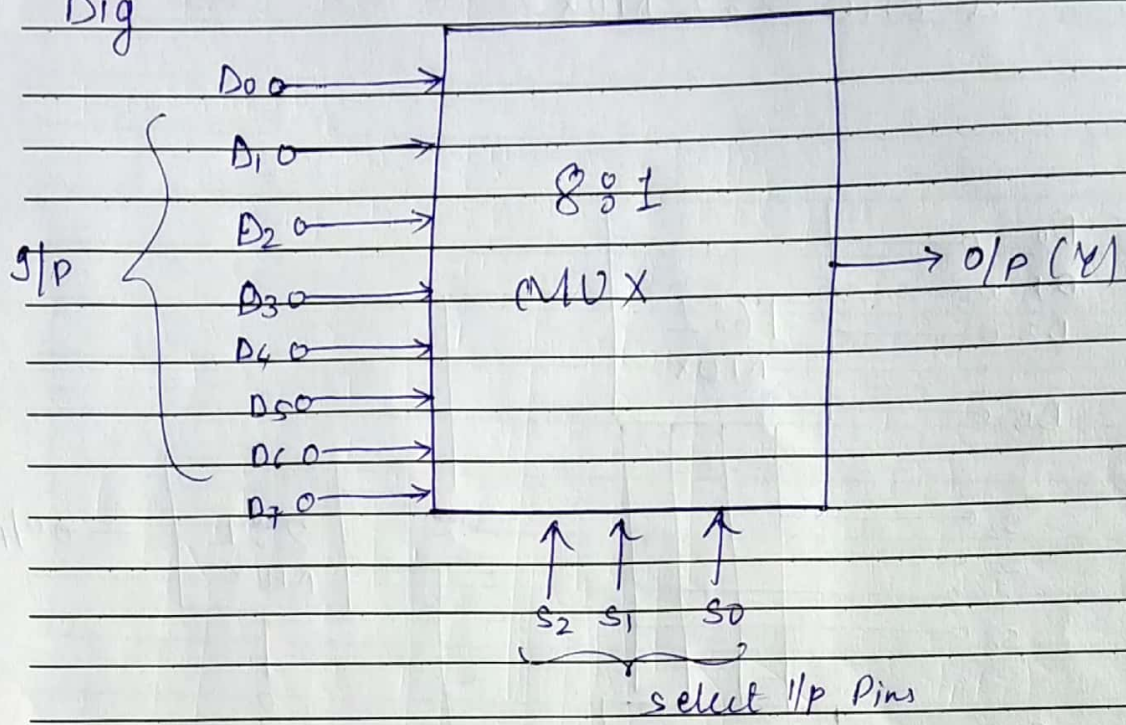
Select Pins			O/P (Y)
S_2	S_1	S_0	
0	0	0	D_{00}
0	0	1	D_{01}
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

Logic dig :

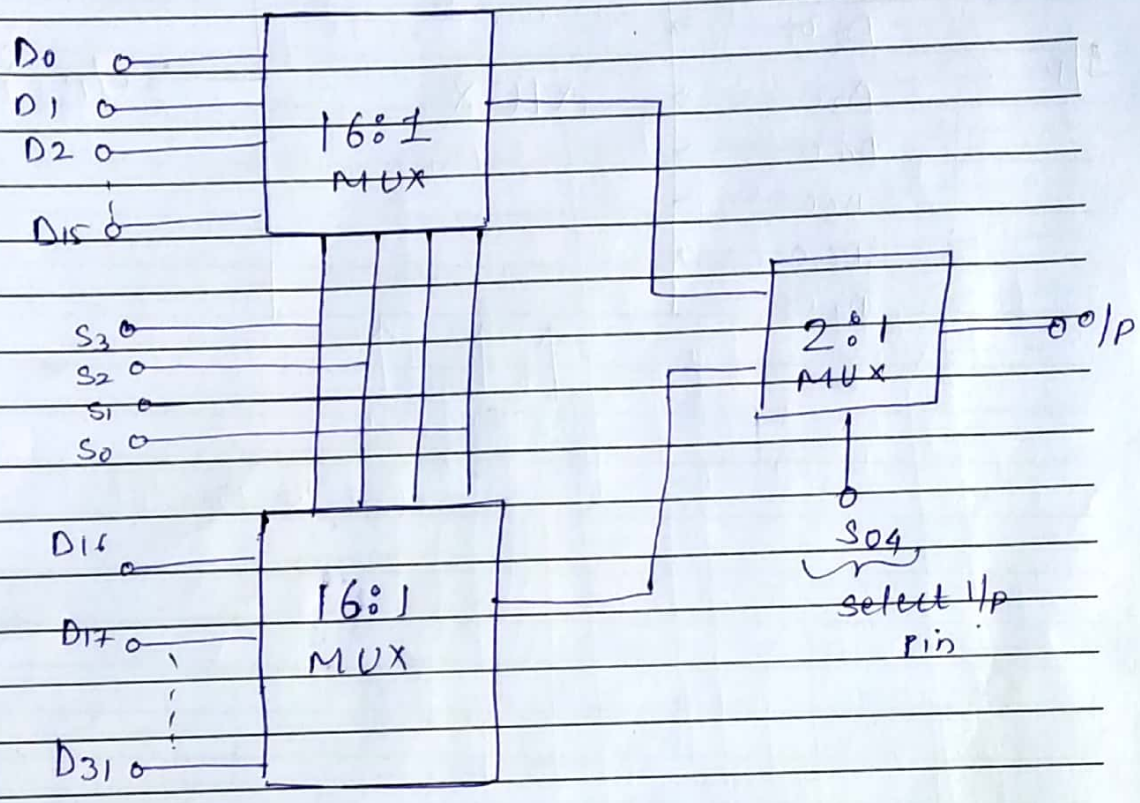


Subject: Name of Faculty: _____

Dig

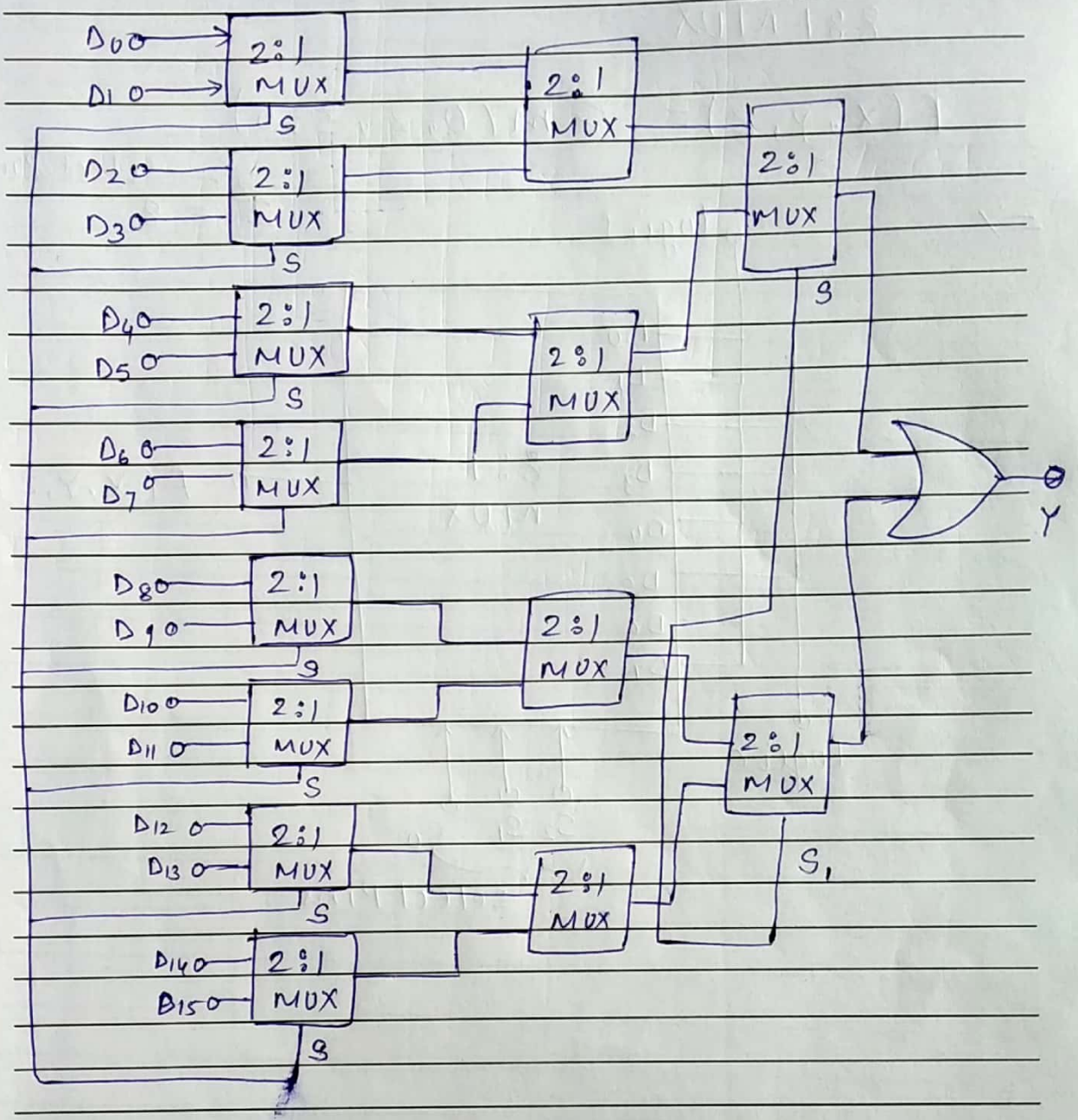


Q Design 32:1 MUX using two 16:1 MUX & one 2:1 MUX



Subject: Name of Faculty:

Q Design 16:1 MUX using 4:1 MUX.



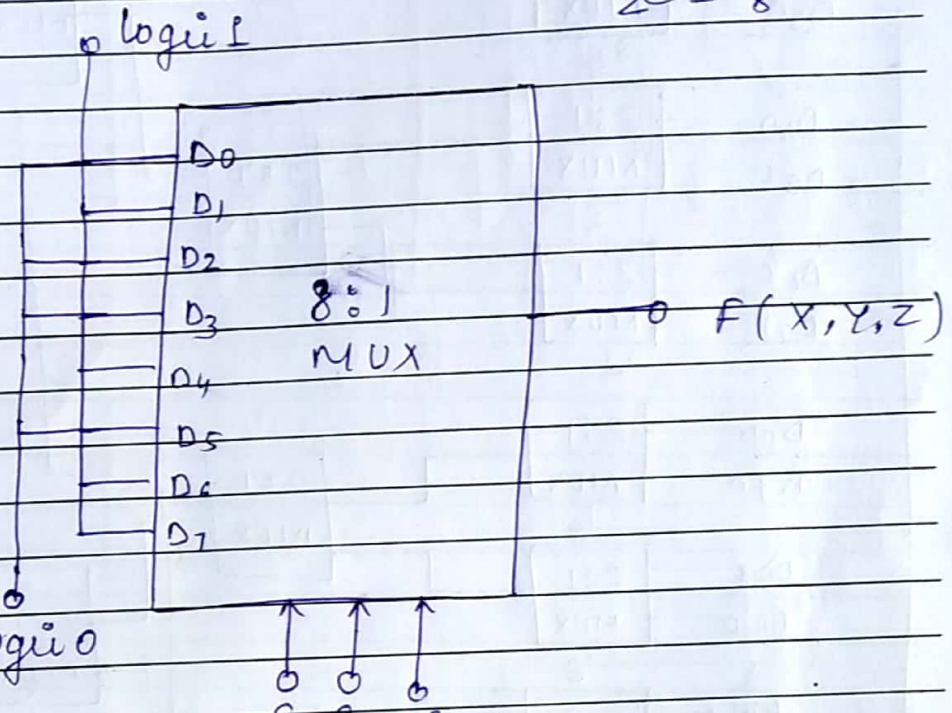
Q Implement the foll function using

8:1 MUX

$F(X, Y, Z) = \Sigma m(0, 2, 3, 5)$

$2^3 = 8$ — select Pins

=>



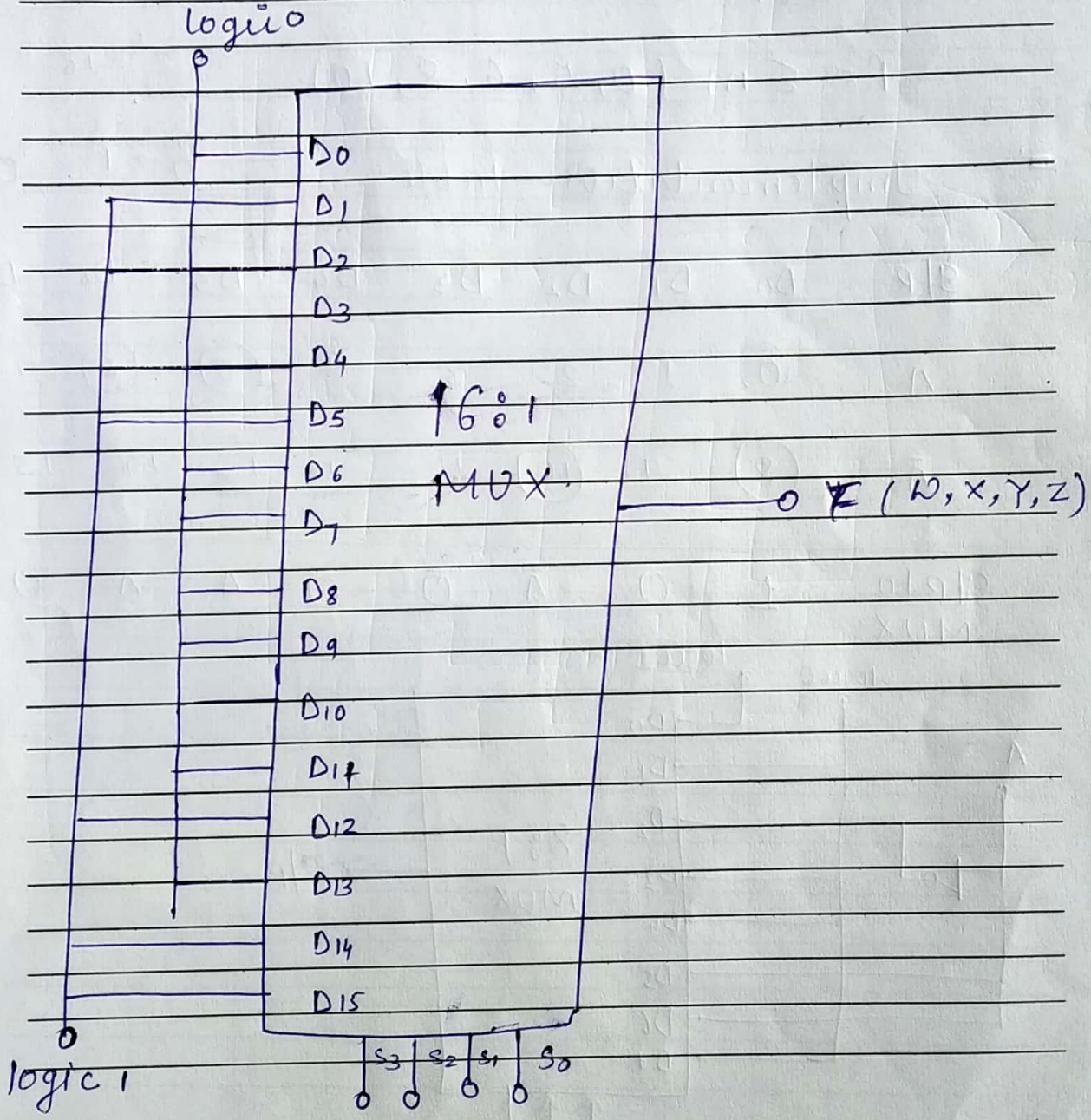
W/12

eg Implement the following function using suitable multiplexer

$f(W, X, Y, Z) = \Sigma M(1, 2, 4, 5, 12, 14, 15)$

Select Pins

$2^4 = 16$ — i/p's



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Q Implement foll function using

$f(A,B,C,D) = \Sigma m\,(1,3,6,5,12,14,15)$

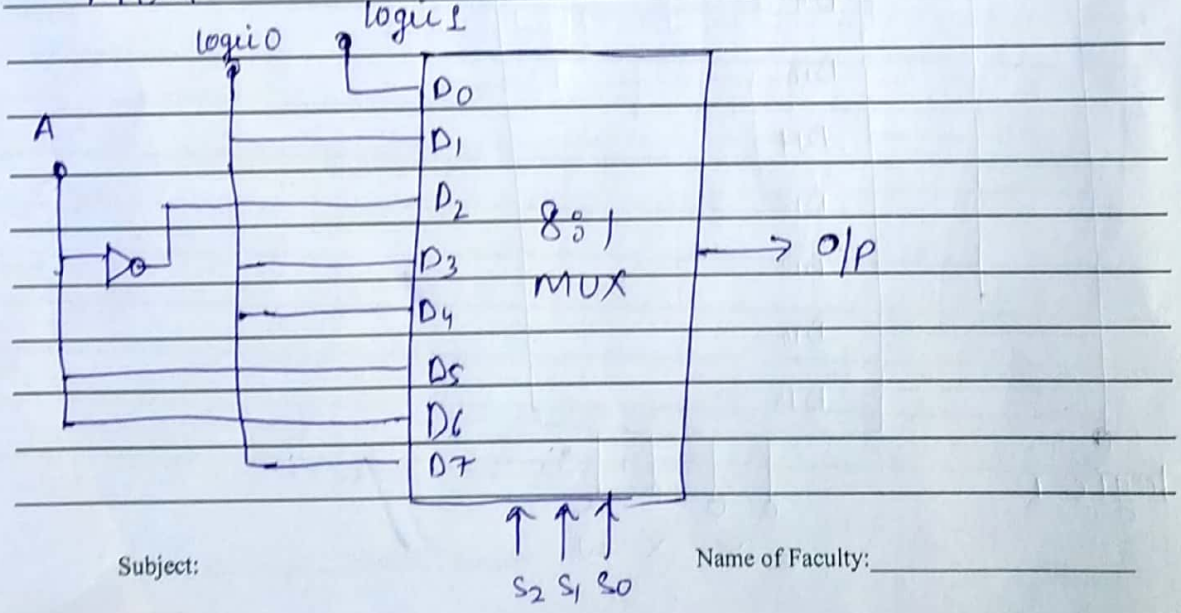
Q Implement the foll function using 8:1 MUX

$f = \Sigma m\,(0,5,6,8,10)$. $2^4 = 16$

$8 \rightarrow 1$ O

⇒ Implementation table.

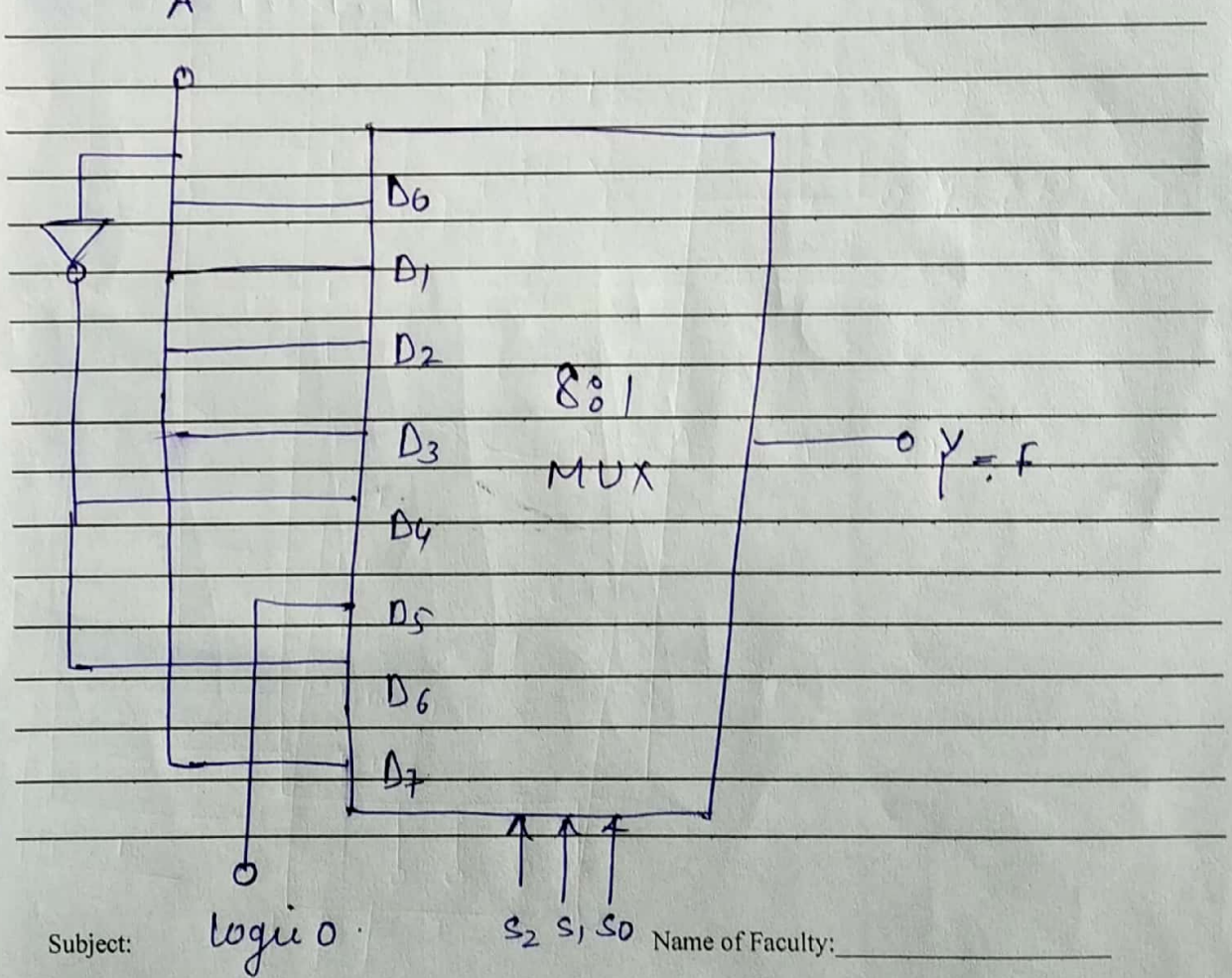
I/P	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
A	(0)	1	2	3	4	(5)	(6)	7
$\bar{A}$	(8)	9	(10)	11	12	13	14	15
I/P to MUX	1	0	$\bar{A}$	0	0	A	A	0



S/16 Q Implement the foll function using 8:1 MUX $F = \Sigma m(0,1,2,3,11,12,14,15)$.

⇒ Implementation table

I/P	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
A	(0)	(1)	(2)	(3)	4	5	6	7
$\bar{A}$	8	9	10	11	(12)	13	(14)	(15)
I/P to MUX	A	A	A	A	$\bar{A}$	0	$\bar{A}$	$\bar{A}$



Q Implement the logic function

$f(A,B,C) = \Sigma m(0,3,4,6,7)$

using 4:1 MUX

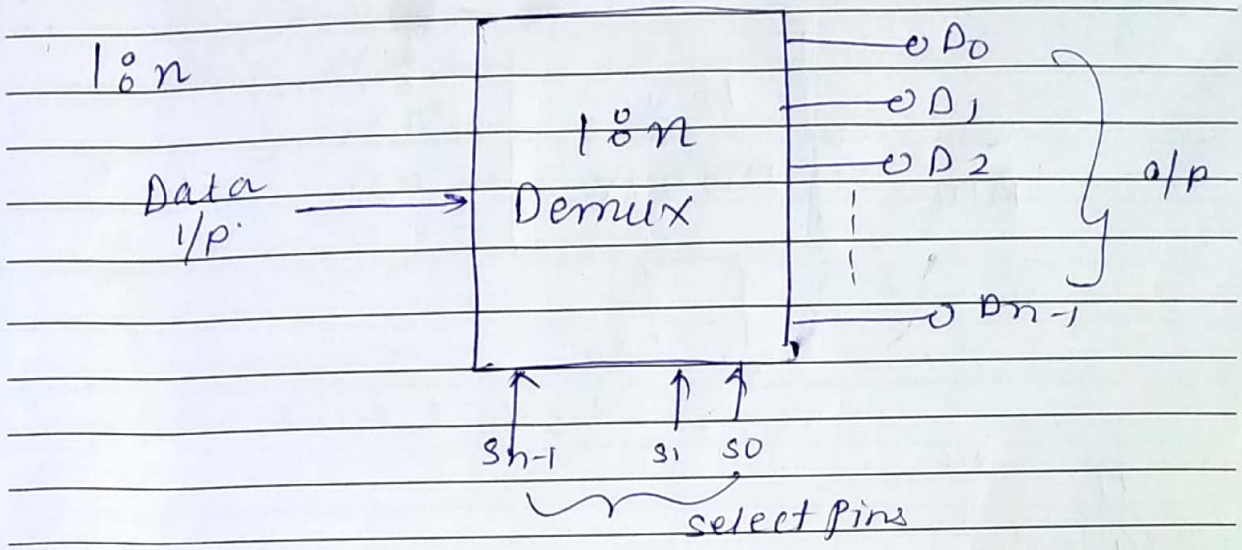
Q Implement full function using 8:1 MUX

$f = \Sigma m(0,1,2,3,11,12,14,15)$

Q Implemnt using 8:1 MUX

$f(A,B,C,D) = \Sigma m(2,4,6,7,9,10,11,12,15)$

⊙ Demultiplexer (Demux).



1) A multiplexer text several i/p & transmit one of them to the o/p. A demultiplexer perform reverse operation

2) A demultiplexer can though as distributor

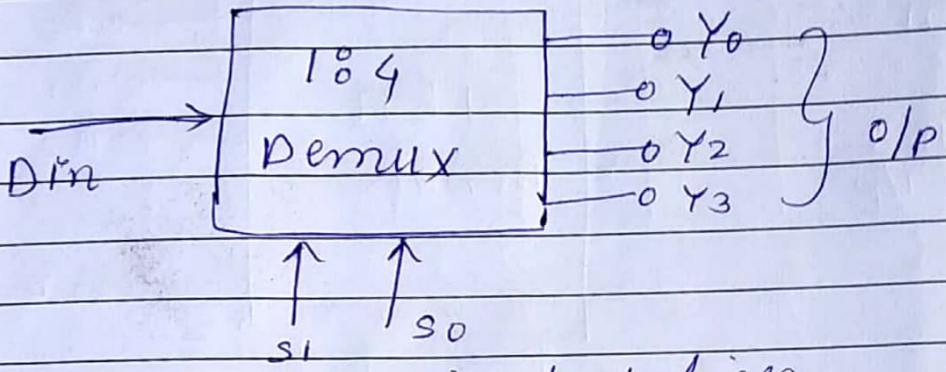
3) The select input determine to which o/p data input will be transmitted

4) The no of o/p lines are "n" and no of select lines are m where

$$n = 2^m$$

This no can also be used as asr binary to decimal with binary i/p applied at select i/ps lines & output will be obtain & corresponding line

1) 1:4 demux



$n = 2^m$

O/P (4) $= 2^2$

$m = 2$

Truth table

Select I/P		O/P			
S_1	S_0	Y_0	Y_1	Y_2	Y_3
0	0	Din	0	0	0
0	1	0	Din	0	0
1	0	0	0	Din	0
1	1	0	0	0	Din

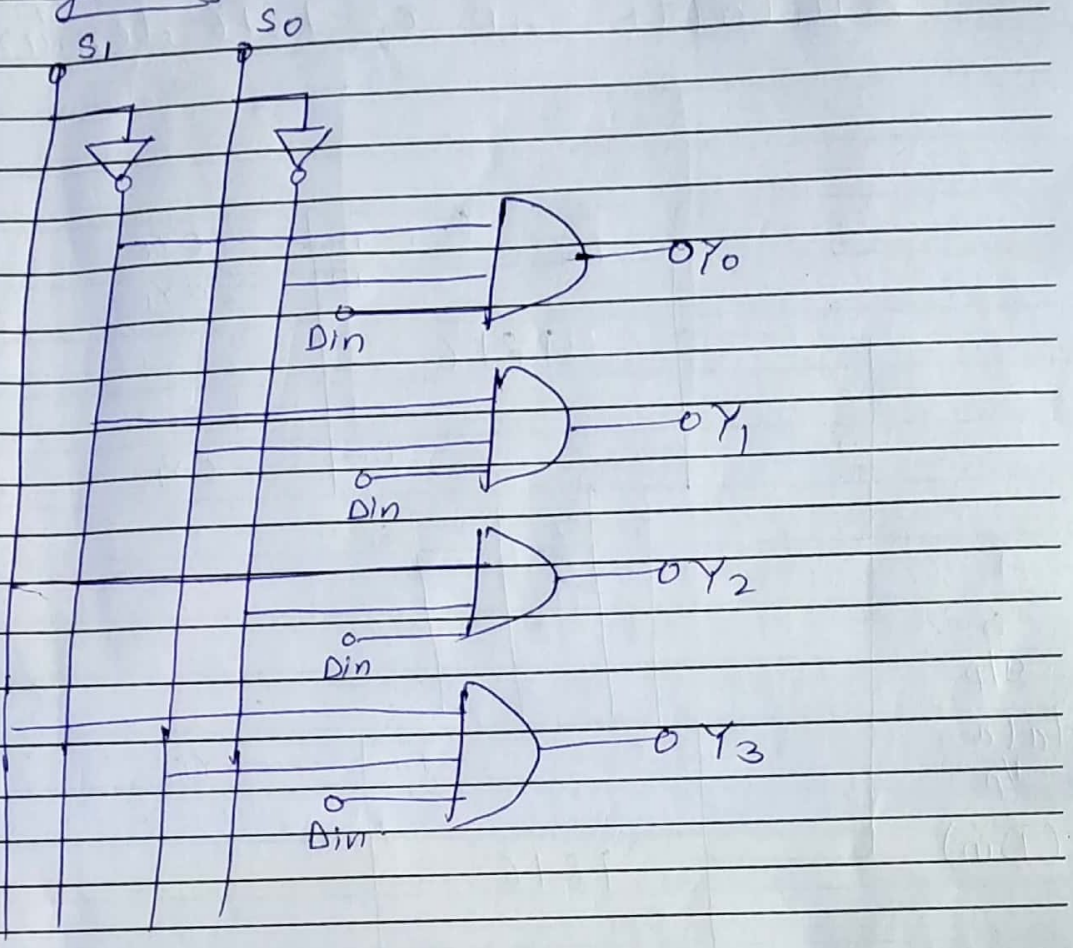
$Y_0 = \bar{S}_0 \bar{S}_1 Din$

$Y_1 = S_0 \bar{S}_1 Din$

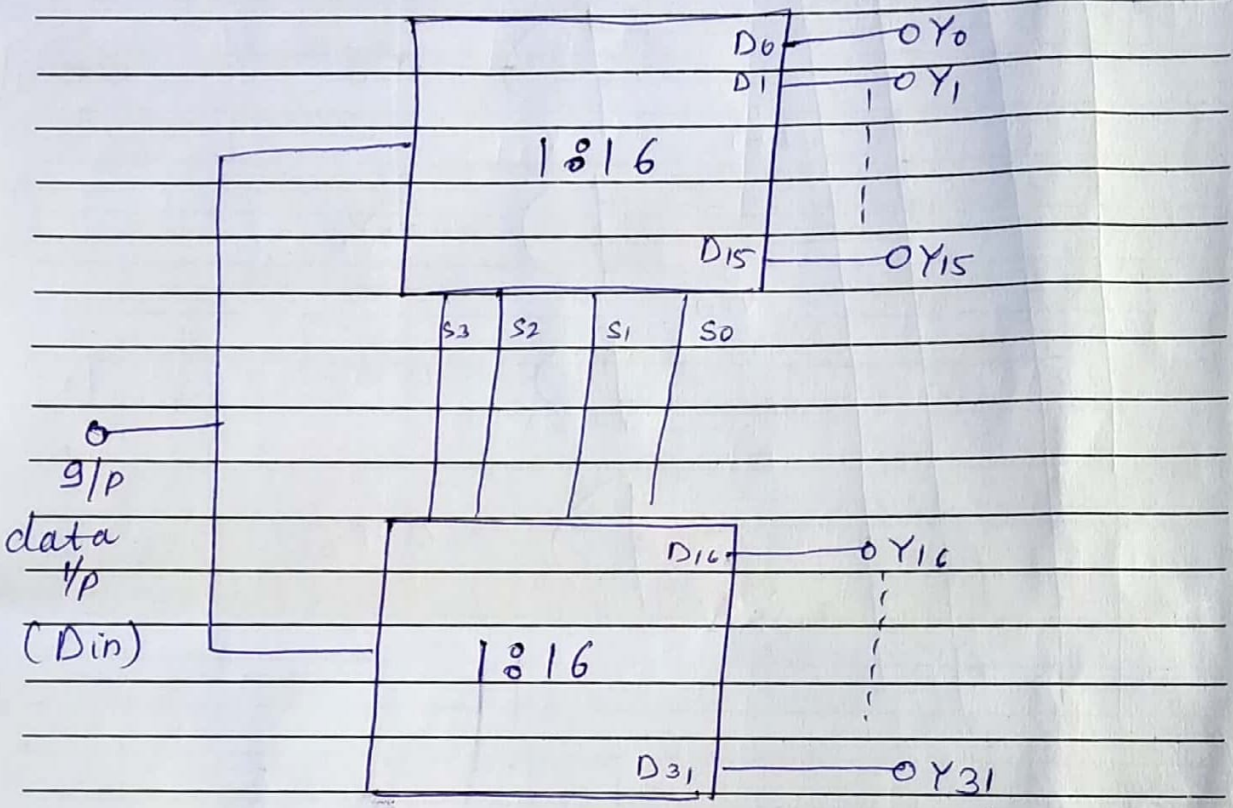
$Y_2 = S_1 \bar{S}_0 Din$

$Y_3 = S_1 S_0 Din$.

Logic dig



Q Obtain 1:32 demux using suitable no of 1:16 demux.



$n = 2^m$

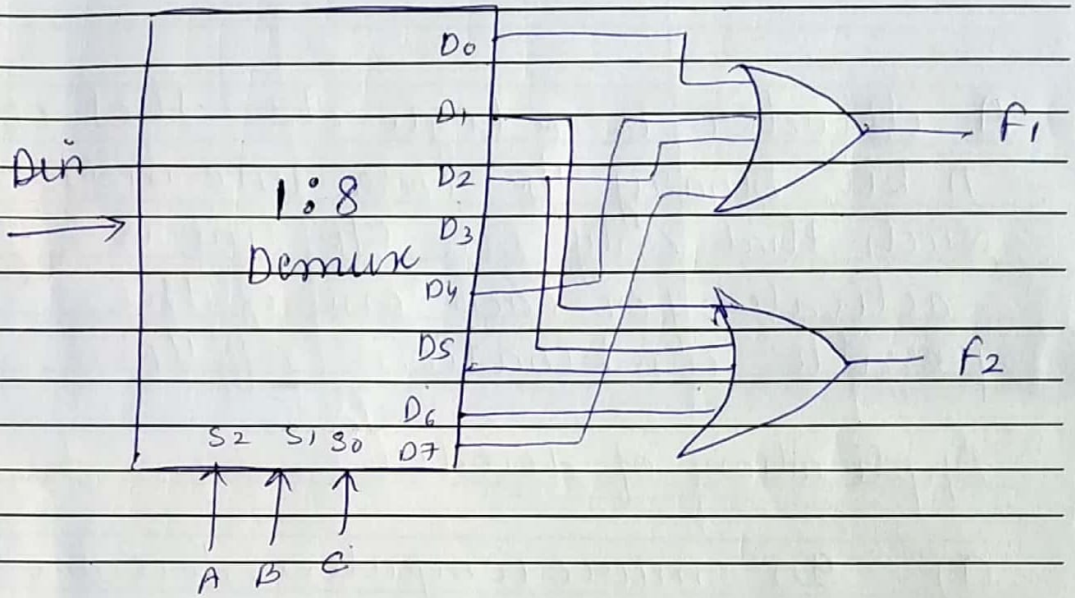
16 = $n = 2^{(4)}$ — seled I/P Pins

O/P

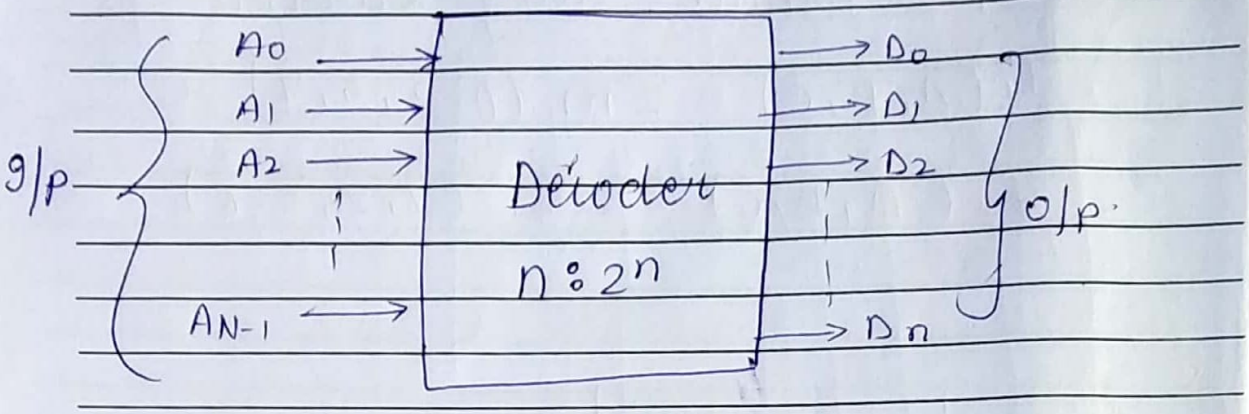
Q8 Realise the foll function using 1:8 Demux using suitable gates

$f_1(A,B,C) = \Sigma m(0,2,4,7)$ &

$f_2(A,B,C) = \Sigma m(1,2,5,6)$



⑥ Decoder



A decoder is a logic ckt that convert n bit binary I/P code into m O/P lines such that only one O/P line is activated for each one of the possible combinations of I/Ps.

Application of decoder

(1) In micro computers, decorder are use for generating chip select signal for selecting a particular memory bank.

(2) In microprocessor, decorders are use for instruction decoding purpose.

Q8 Implement a full adder using 3:8 decorder

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

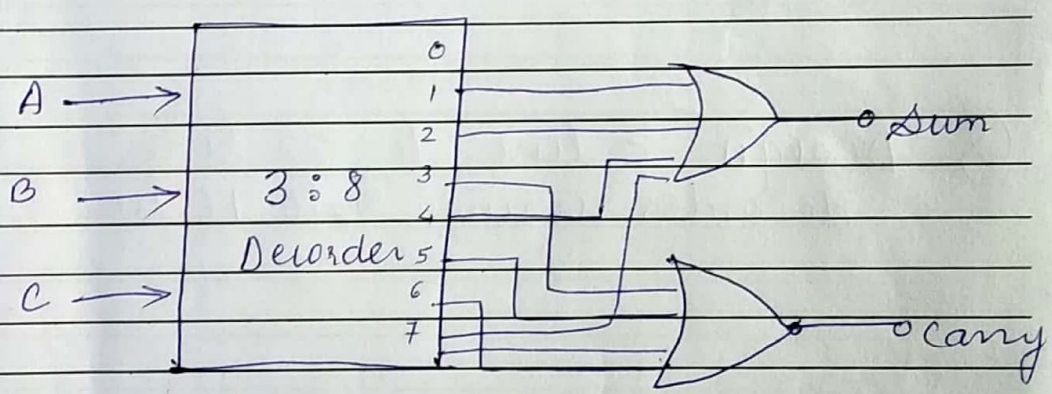
0+0=0

0+1 = S=1, C=0

1+1 = S=0, C=1

Sum = Σm(1,2,4,7)

Carry = ΣM(3,5,6,7).

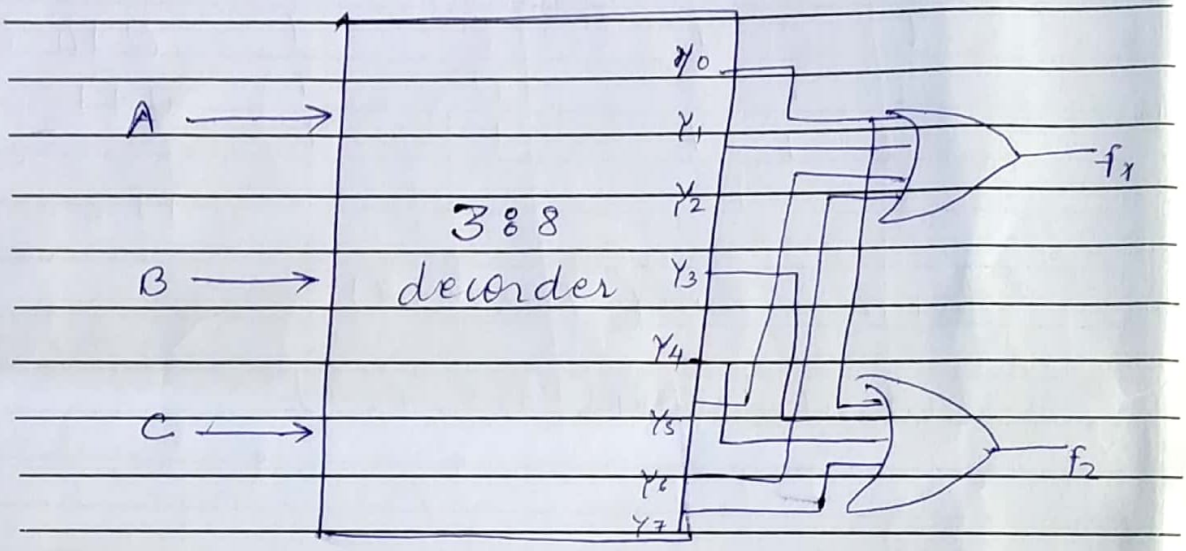


Subject: Name of Faculty:_____

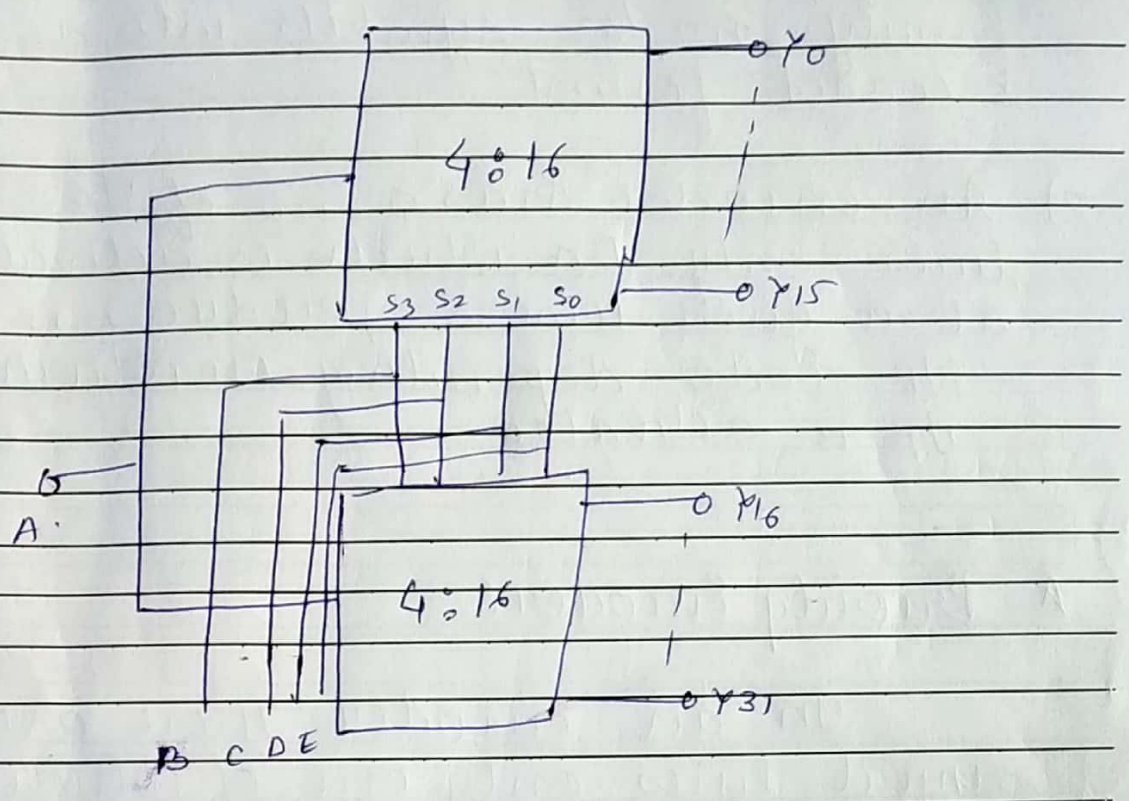
Q. Implement using 3:8 decoder

$f_1(A,B,C) = \Sigma m(0,1,5,6)$

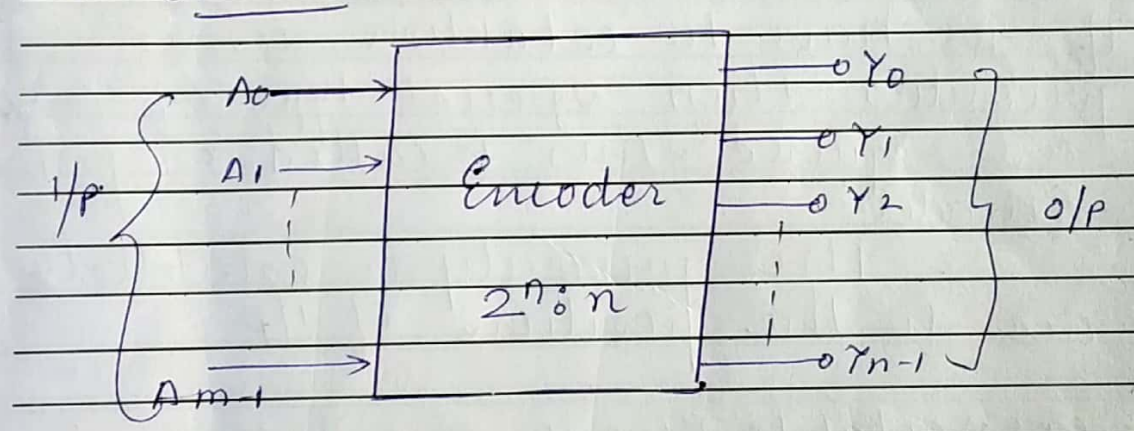
$f_2(A,B,C) = \Sigma m(0,3,4,7)$.



Q. Design 5 line to 32 line decoder using 4 to 16 line



★ Encoder



An encoder is a combinational ckt which is design to perform the inverse operation of decoder

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Encoding is process of converting family no ar symbols into a coded format.

2) An encoder has a no of i/p lines only On which is activated at a given time & produces n-bit o/p code depending on which i/p is activated.

* Priority Encoder:

In an encoder there are n input lines only one of which is active in case if more than one i/p are active & at the same time if we have to establish some priorities then special type of encorders are required. This is called as priority Encoder.

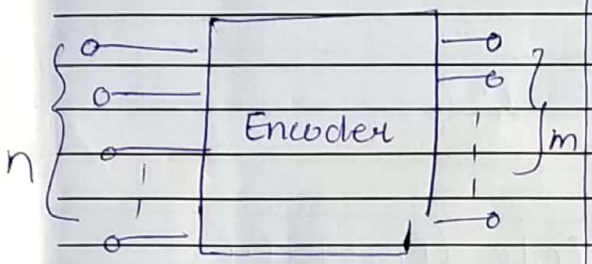
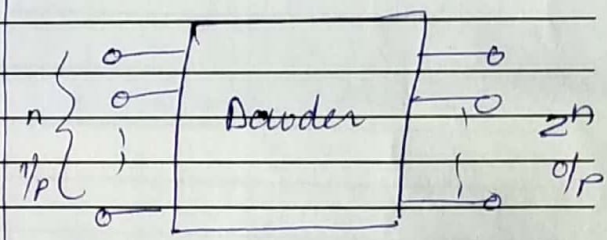
The priority is establish acc to the position of i/p

eg: 1) octal to Binary priority encoder.

2) Decimal to BCD priority encoder

3) Hexadecimal to Binary

Q Difference beth Decoder & Encoder

Encoder	Decoder.
1] It is one which generates binary code from numerous alphabate & characters	1) It is one which generates more compact codes to a less compact codes
2) It has N no of i/p lines & m no of o/p lines	2) It has N i/p & max 2^n o/p
3) Block dig of it 	3) Block dig 
4) Eg 1) Priority Encoder 2) Hexadecimal to Binary encoder	4) Eg 1) code converters 2) BCD to 7 segment decoders

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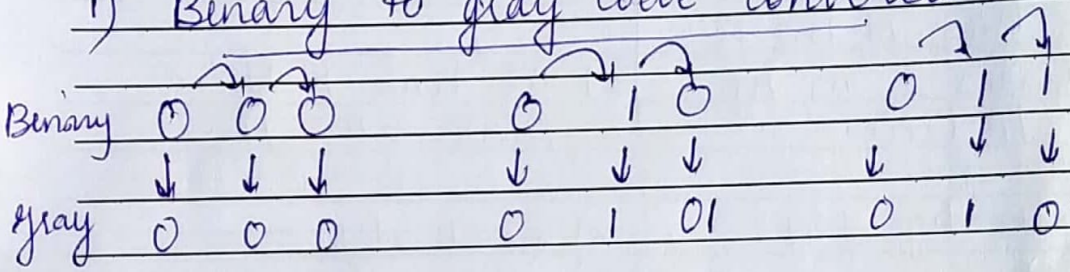
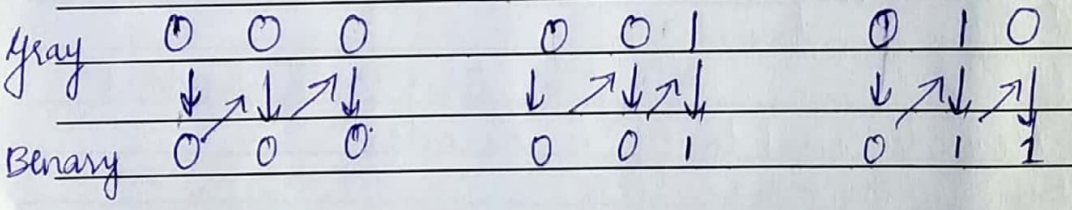
✱ Code Converters

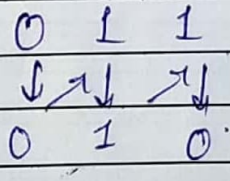
Code Converter are usually multiple o/p ckt. Thus a code converter is a logic ckt whose i/p are bit patterns representing no or one code & whose o/p are the corresponding in different code

1) Binary to gray code Conversion



2) Gray to Binary Code Conversion



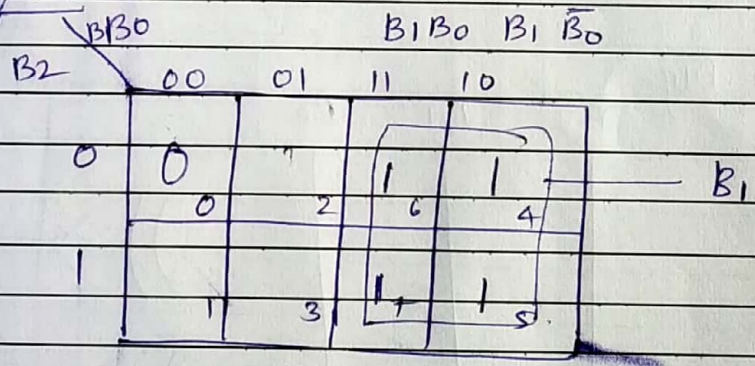


** Design 3 bit binary to gray code converter using suitable gates

⇒ Truth Table

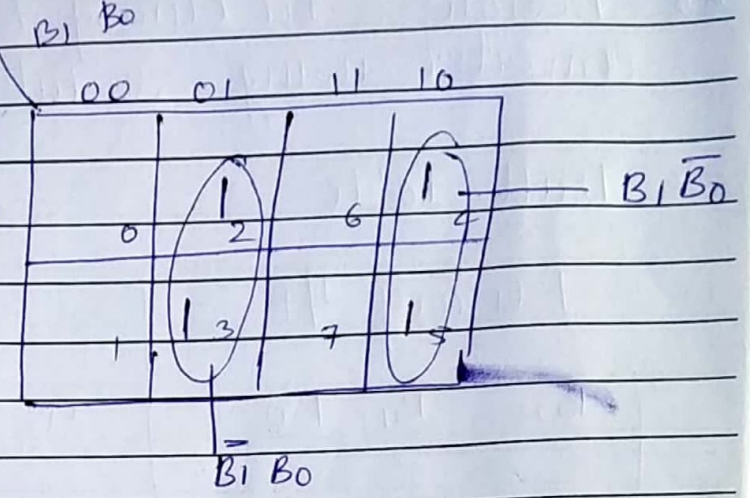
	Binary I/P			Gray O/P		
	B_2	B_1	B_0	G_2	G_1	G_0
0	0	0	0	0	0	0
1	0	0	1	0	0	1
2	0	1	0	0	1	1
3	0	1	1	0	1	0
4	1	0	0	1	1	0
5	1	0	1	1	1	1
6	1	1	0	1	0	1
7	1	1	1	1	0	0

K-Map for G_2



$G_2 = B_1$

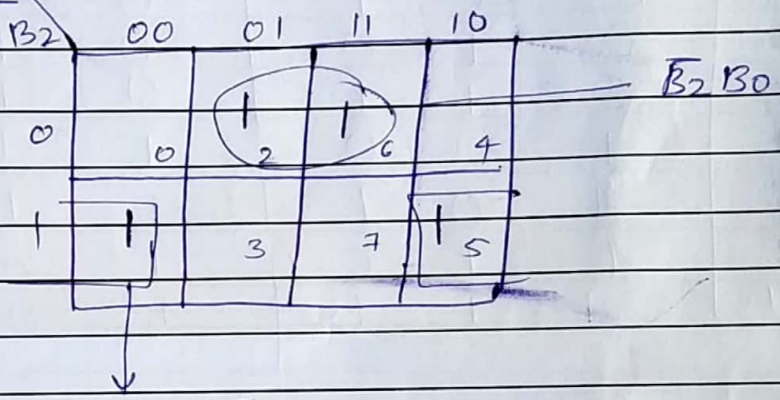
Kmap for G_1



$G_1 = \bar{B_0} B_1 + B_0 \bar{B_1}$

$= B_0 \oplus B_1$

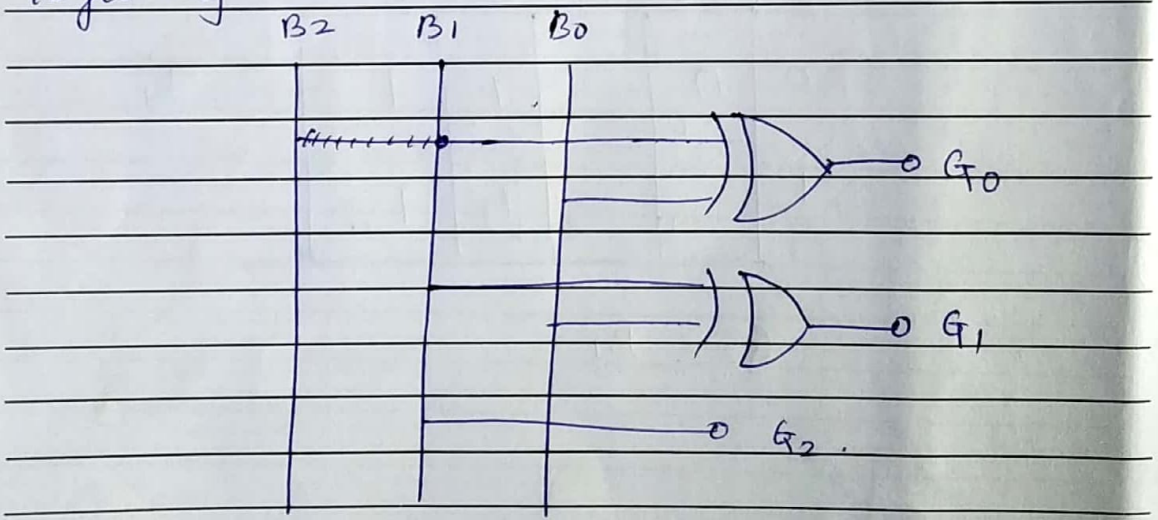
Kmap for G_0



$G_0 = B_0 \bar{B_2} + B_2 \bar{B_0}$

$= B_0 \oplus B_1$

logic Dig:



** 0 to 9

Q Design BCD to Excess 3 code Converter using minimum no of NAND gate.

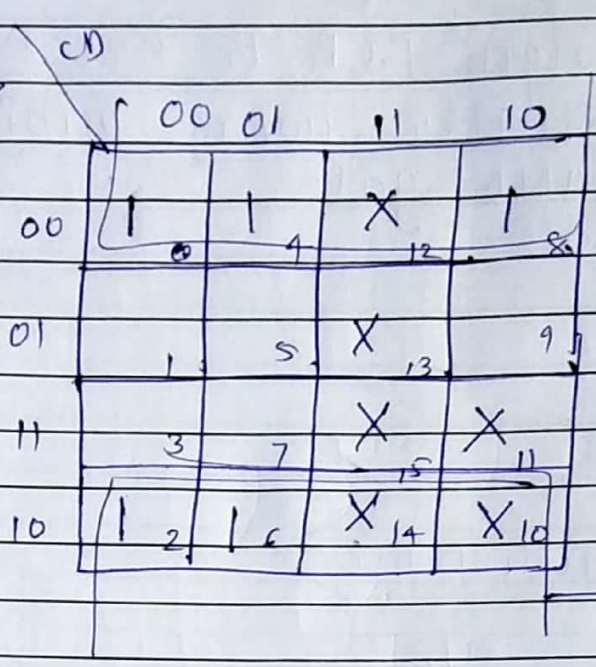
8421
0000
0011
0011
+0011
0100

Truth Table:

	I/P BCD				O/P Excess-3			
	A (8)	B (4)	C (2)	D (1)	W	X	Y	Z
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0
~~10~~								

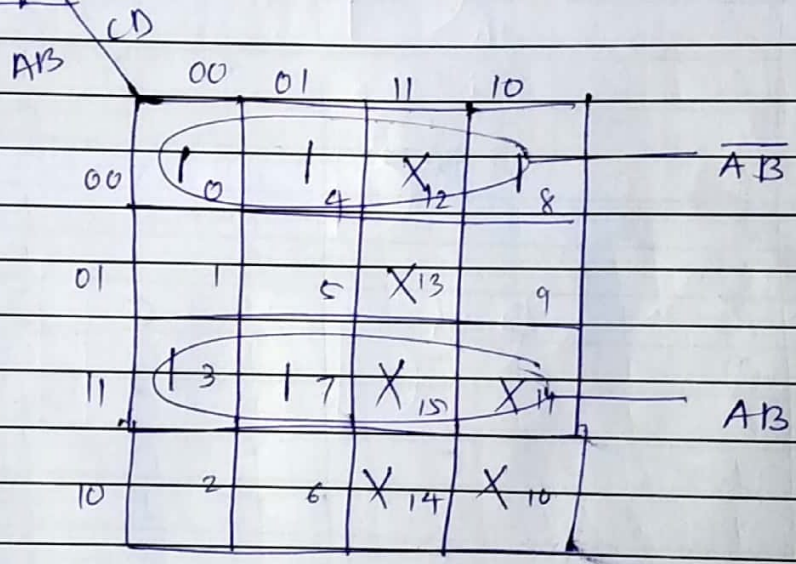
The I/P conditions M_{10}, M_{11}, M_{12}, M_{13}, M_{14}, M_{15} are don't care condition

Kmap for Z



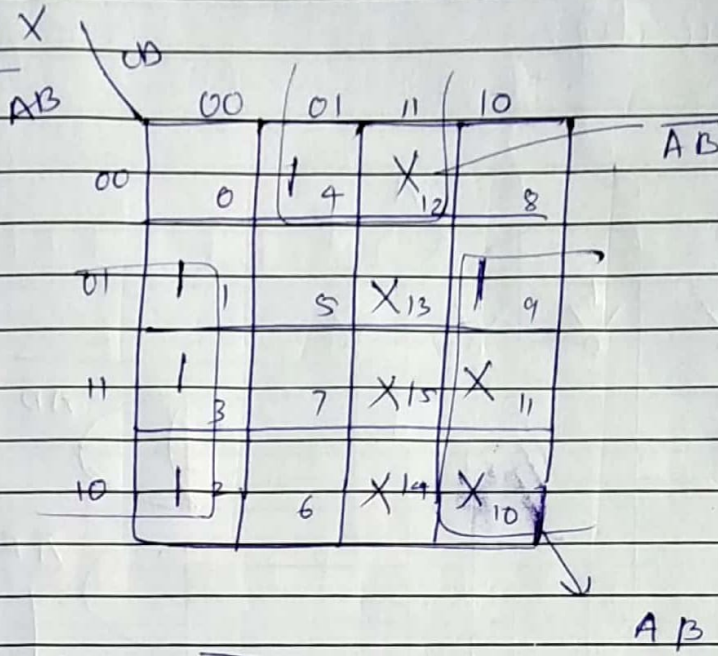
$Z = \bar{B}$

K-map for Y



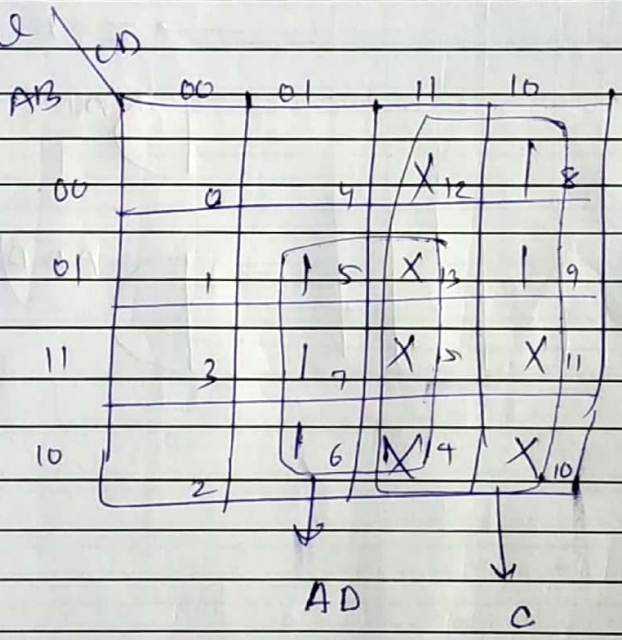
$Y = AB + \bar{A}\bar{B}$

Kmap for X



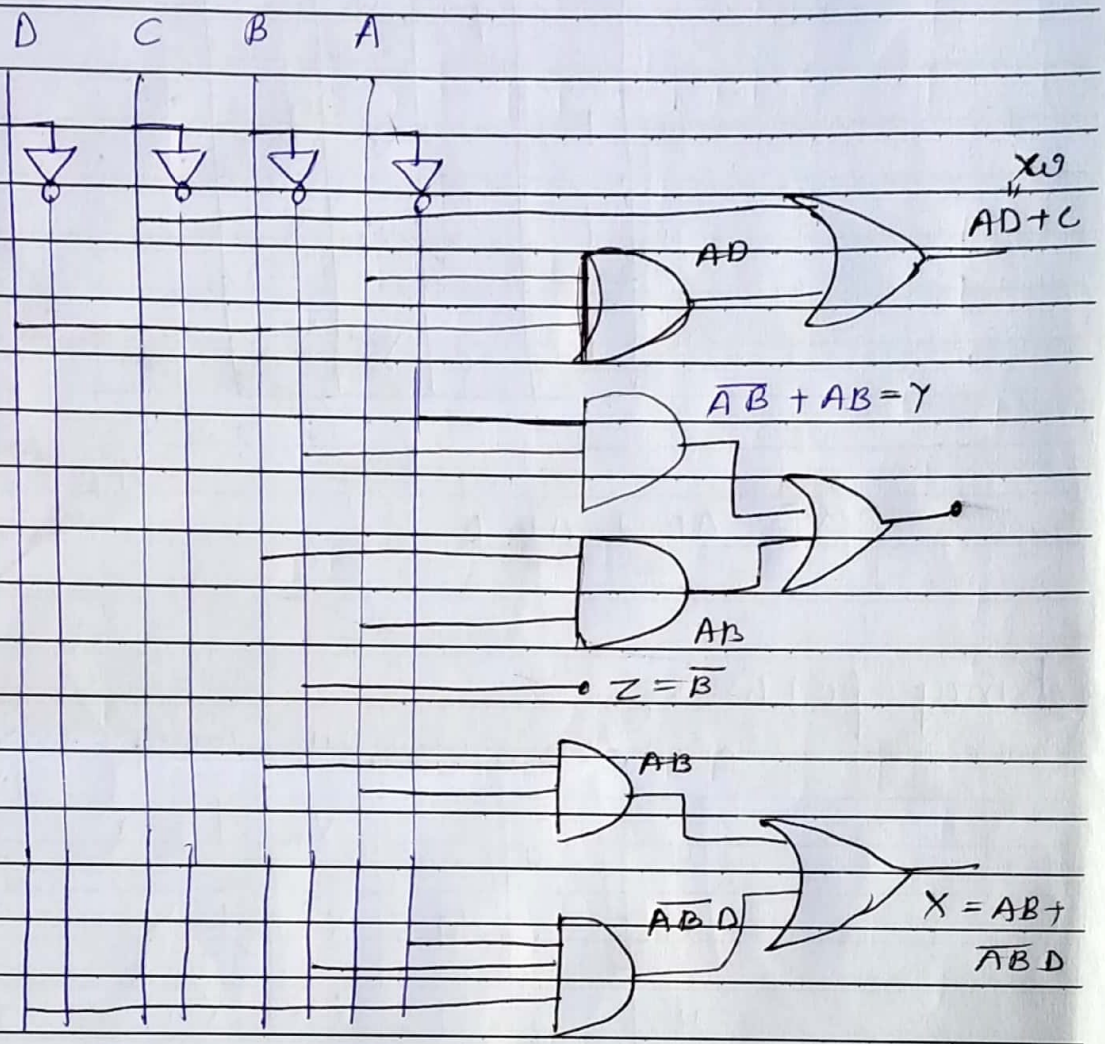
$X = AB + \overline{A}\overline{B}D$

Kmap for W



$W = AD + C$

logic dig:



Q. Design a BCD to 7 segment decoder for common cathode Configuration

In this decorder the o/p are used to drive 7 segment display. the seven segment is one of the common use display

The calculator, use BCD no which are converted into 7 segments code with the help of combinational logic ckt

The seven segment a, b, c, d, e, f, g are shown in foll figure

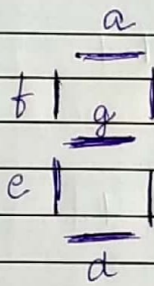
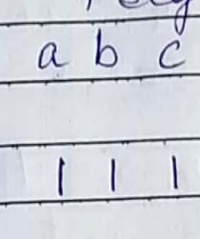
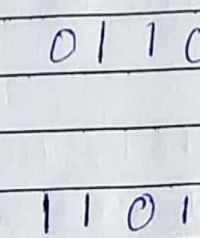
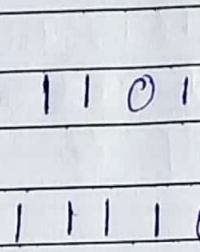
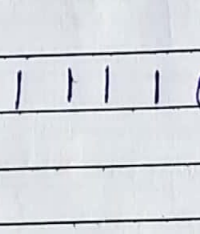
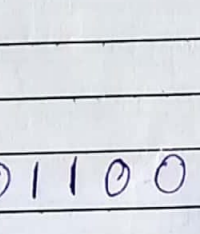
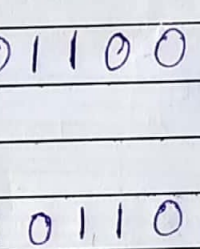
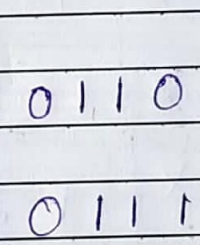
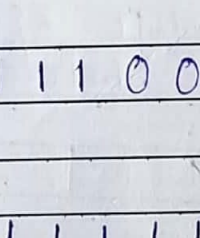
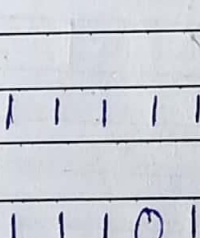


Fig: seven segment display

The truth table of seven segment is shown below

Truth table

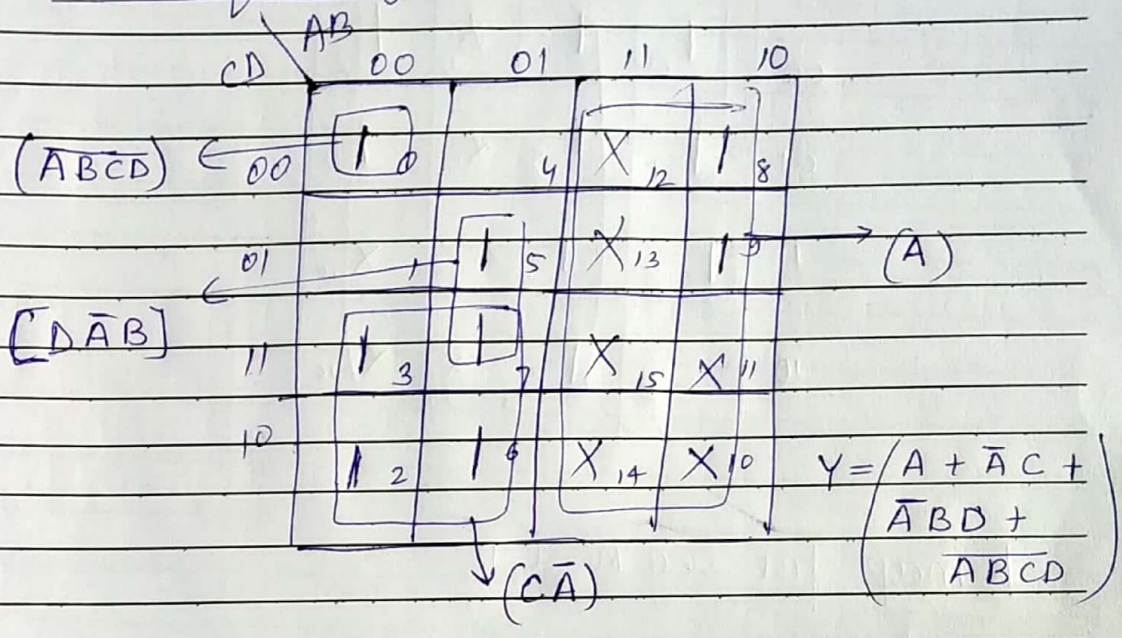
Decimal no	I/Ps A	B	C	D	7 Segments a	b	c	d	e	f	g	Display
0	0	0	0	0	1	1	1	1	1	1	0	
1	0	0	0	1	0	1	1	0	0	0	0	
2	0	0	1	0	1	1	0	1	1	0	1	
3	0	0	1	1	1	1	1	1	0	0	1	
4	0	1	0	0	0	1	1	0	0	1	1	
5	0	1	0	1	1	0	1	1	0	1	1	
6	0	1	1	0	1	0	1	1	1	1	1	
7	0	1	1	1	1	1	1	0	0	0	0	
8	1	0	0	0	1	1	1	1	1	1	1	
9	1	0	0	1	1	1	1	1	0	1	1	

Subject: Name of Faculty:_____

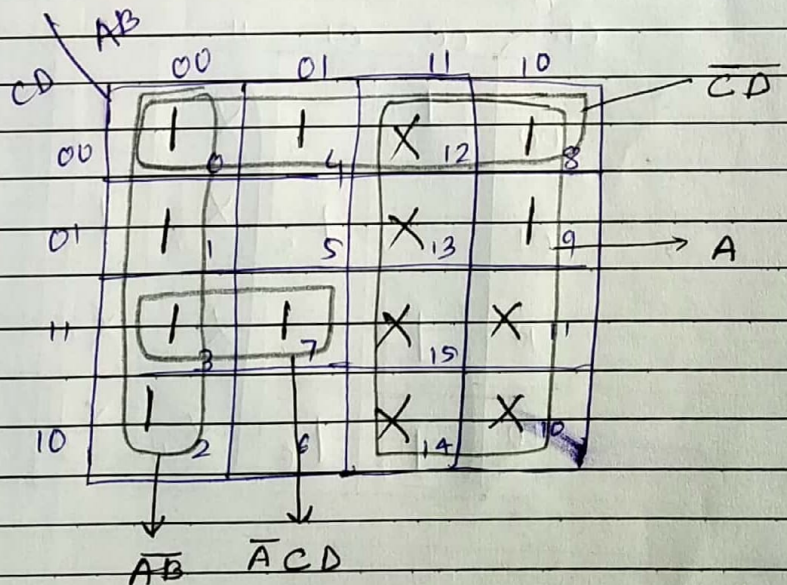
TGPCET Department of_____

K map for 7 segment a, b, c, d, e, f, g is function of A, B, C, D

K-map for segment a



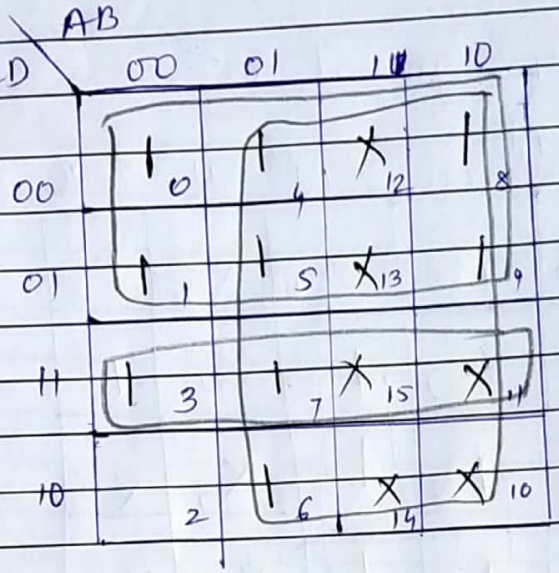
K map for segment b



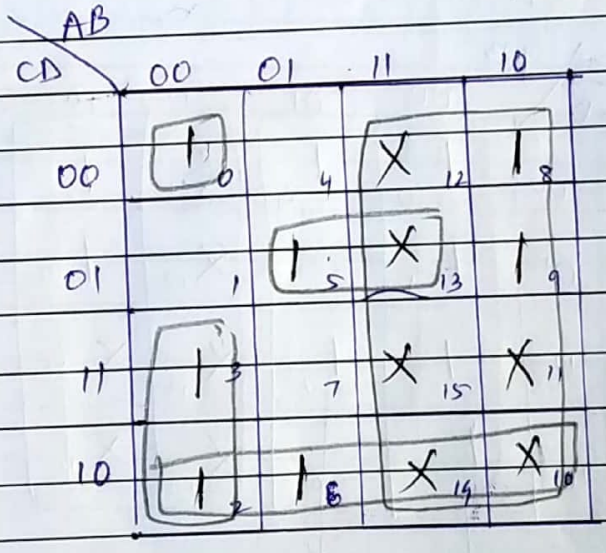
$$B = A + \overline{C}\,\overline{D} + \overline{A}\,\overline{B} + \overline{A}CD$$

Subject: Name of Faculty:_____

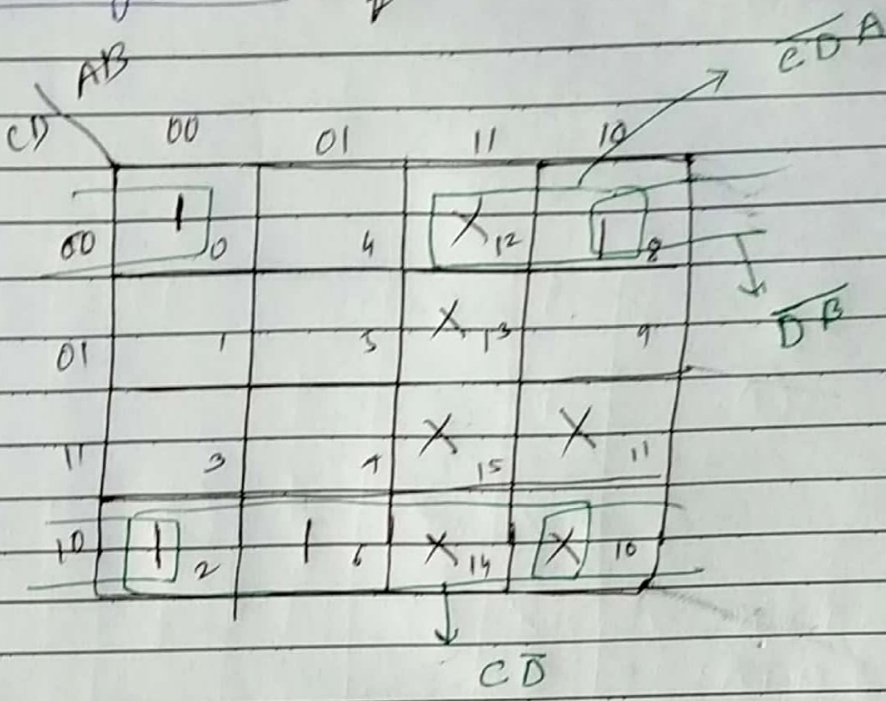
K map for Segment C



K map for segment D



K map segment E



K map for segment f